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Product Evaluation Report

TCC 244, 256 X 4, 1K CMOS Random Access Memory (RAM)

S. F. Suszko

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National Aeronautics and
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Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

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Product Evaluation Report

TCC 244, 256 X 4, 1K CMOS Random Access Memory (RAM)

S. F. Suszko

Prepared by:

Stefan F. Suszko

Reviewed by:

Kamal Soliman (MTS),
Memory Devices Specialist

L.M. Hess,
LSI Group Leader

Approved by:

W.R. Scott,
Group Supervisor,
Parts Engineering Group

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California Institute of Technology
Pasadena, California

PREFACE

This evaluation has been performed in order to gain a first-hand knowledge of and insight into this product's inherent material structures and its functions; to assess the relative quality of materials, together with pattern design; and to reveal possible flaws. Subsequently, this report should be useful in the establishment of reliability criteria for this process technology, for related device types, and for analysis of failed parts.

The product evaluation described herein attempts to avoid redundancy and to minimize indirect inferences not drawn directly from observation. Each section is an attempt to deal directly and solely with the subject matter of that section. For the sake of continuity, however, and to gain a more complete insight into this device, extensive use was made of photo figures as "evidential reference" to materials' processes and design patterns.

The work described in this report was performed by Steve Suszko, JPL Parts Engineering, Section 514.

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SECTION I

INTRODUCTION

1.1 DEVICE DESCRIPTION

The Sandia TCC 244 is a 256 x 4 bit (1K), fully static, asychronous Random Access Memory (RAM) chip. It requires no precharge or clocking signal. The 1K memory has eight address input buffers (A_0 - A_7), four data input buffers (DI_0 - DI_3) and four tri-state data output buffers DO_0 - DO_3. The four timing control buffers, $\overline{MWR}$, CS_1, CS_2 and $\overline{MRD}$ provide appropriate timing pulses to enable the binary data in read and write modes through the column sense circuits and tri-state output buffers to be displayed at the output pads DO_0 - DO_3.

The TCC 244 RAM is on N-type bulk silicon and utilizes RCA developed CMOS (C^2L) self-aligned closed polysi-gate process technology. However, this second source TCC 244 CMOS chip is fabricated with radiation hardened proprietary process developed by Sandia Laboratory. The chip two-level interconnect is aluminum and polysilicon with interlevel SiO_2 insulation. The chip is packaged in a 28-pin flat-pack ceramic package with a hermetically sealed metal lid.

The device operating voltage is 4.5 to 5.5 volts. The operating temperatures is -55 to +125°C.

1.2 DOCUMENT USES

Two devices were submitted for product evaluation by K. Soliman, JPL Memory Specialist. The devices were photographed for identification as shown in Figures 2-1 and 2-2.

For detailed information see: Section III, Electrical Design Evaluation; Section IV, Materials Evaluation; Section V, Process Fabrication; and Appendix A, Electrical Ratings.

SECTION II
EXTERNAL EXAMINATION

2.1 EXTERNAL VISUAL INSPECTION

The two devices were examined per MIL-STD 883B, Method 2009.1 for integrity of package seal, lead terminals and any evidence of damage. The package markings are identified on the metal lids and on the bottom as shown in Figures 2-1 and 2-2.

2.2 DIMENSIONS

Package Dimensions	(mils)	(mm)
Length:	0.717	18
Width:	0.650	16
Thickness with lid:	0.115	3

Lead Dimensions		
Length:	0.335	8.5
Width:	0.022	0.78
Thickness:	0.0065	0.18
Pin spacing:	0.050	1.12

2.3 HERMETICITY TEST

The devices were placed in a helium pressure container with pressure set at 35 psi (He) for an 18 hour duration. Fine and gross leak tests were performed within 30 minutes after removal of the two devices from the container per MIL-STD 883B, Method 1014.2.

The gross leak test was performed in fc-43 (fluor-carbon) liquid at +125°C. Results: No leaks were observed.

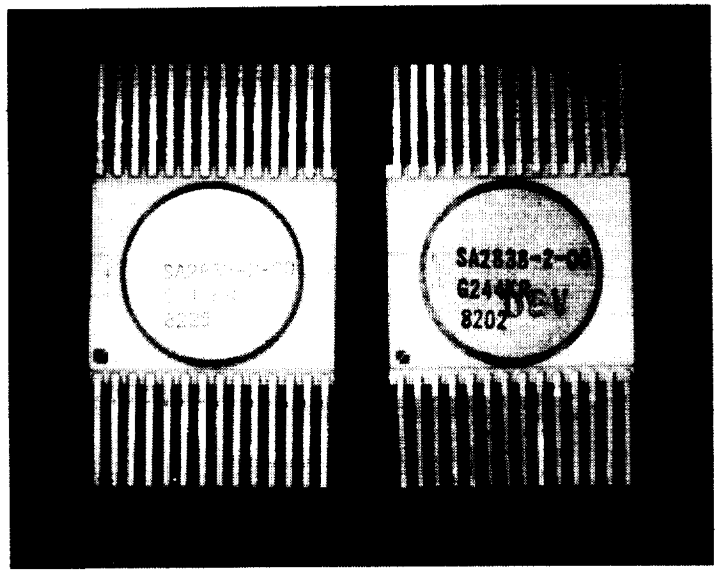


Figure 2-1. 1.8x top view of two devices with markings on metal lids.

Figure 2-2. Bottom view of the same two devices.

2.4 X-RAY RADIOGRAPHY

X-ray photographs of each package cavity show a gold eutectic die attach with numerous voids beneath each chip, a feature which may be a cause of thermal problems in the functional use of the devices. (See Figures 2-3 and 2-4.)

2.5 INTERNAL EXAMINATION: DELIDDING

The two devices were delidded on a wet sanding disk by grinding off the metal lid to the thinness which made it possible to peel the metal off with an X-Acto knife.

Figure 2-5 shows the two delidded devices with die cavities exposed.

Figure 2-6 shows the magnified package cavity, a chip with wire bonds to the package lead frame and an outline of a gold eutectic die attach material.

2.6 OPTICAL AND SEM EXAMINATION AFTER DELIDDING (Before protective passivation removal.)

The exposed die cavity of each device was examined, both with an optical microscope and with a Scanning Electron Microscope (SEM) in order to determine the quality of workmanship, assembly technique and cleanliness, per MIL-STD 883B, Method 2010.3. The die passivation, wire-to-die and package lead frame and die attach fillet were inspected.

Optical Figure 2-7 shows a magnified view of a passivated memory chip with metallization, interconnect pattern only and die pads with wire bonds. Optically, the opacity of protective passivation with sandy gradularity makes the examination of chip patterns difficult to define. SEM inspection and X-ray spectroscopic analysis identified the die attach material to be gold eutectic, however the die attach was found to be inadequate.

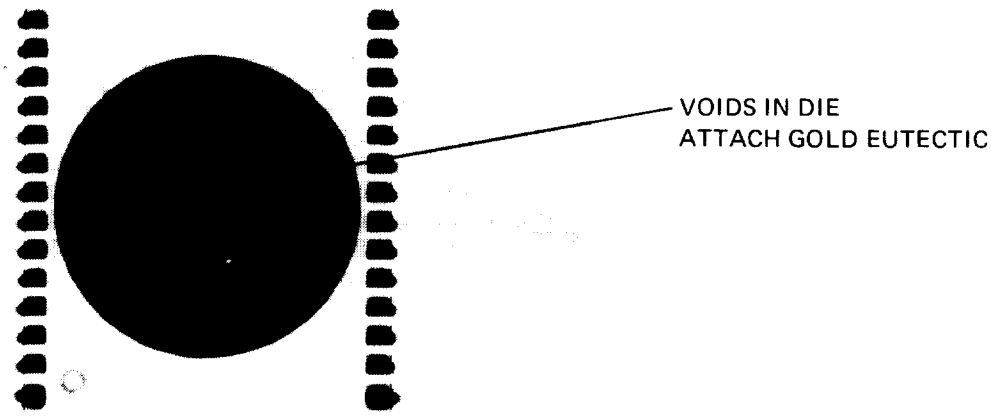


Figure 2-3. 2.8x magnified X-ray view of device 1, top-side with outline of die attach and lead frame. Note void pattern in die attach.

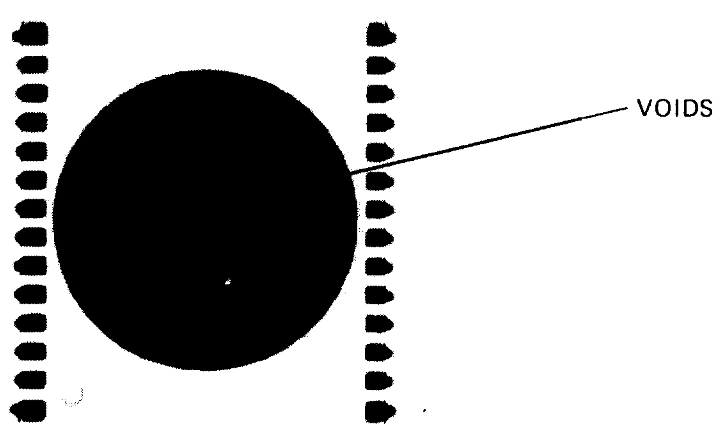


Figure 2-4. X-ray view of device 2. Note die attach voids.

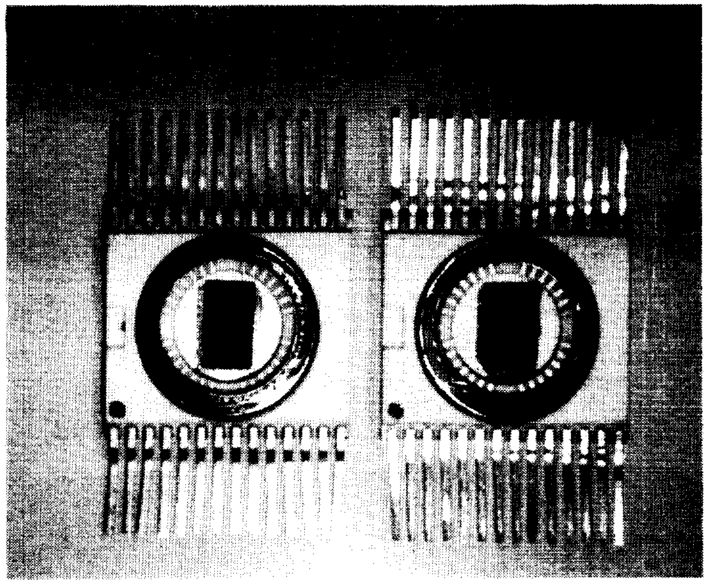


Figure 2-5. 1.8x optical view of two delidded devices with opposed chip and lead frame cavity.

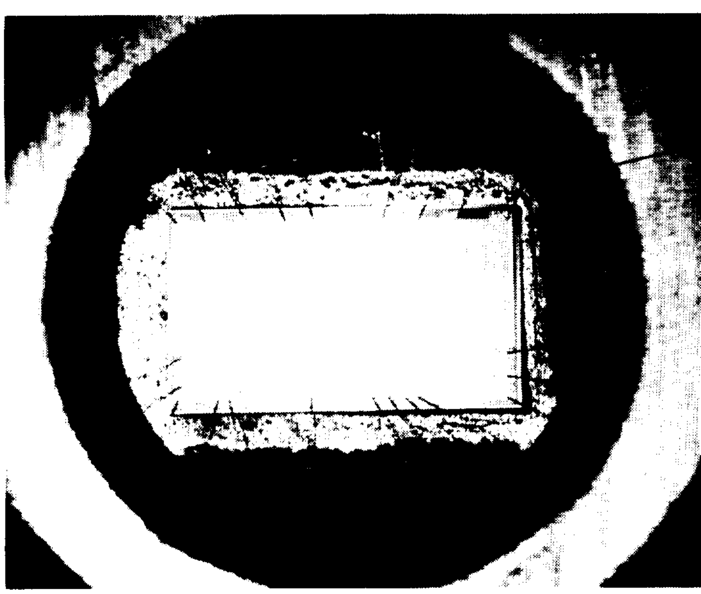


Figure 2-6. Magnified optical view of package lead frame, cavity with die attach outline and die with wire bonds.

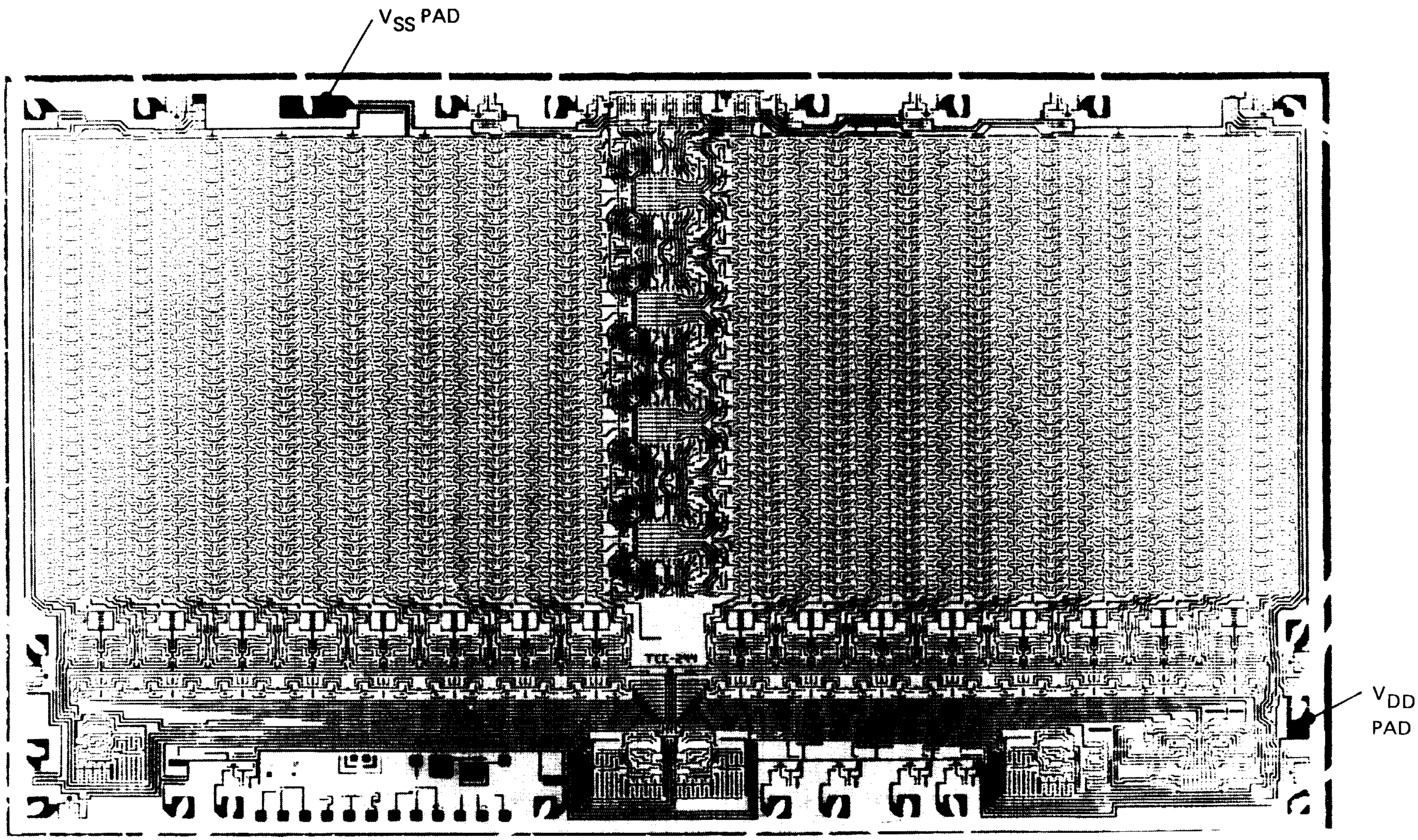


Figure 2-7. 40x magnified optical view of TCC 244 1K CMOS chip metal interconnect mask.

SEM Figures 2-8 and 2-9 show corners of each chip with saw and break slicing method and a poor (missiing) die fillet at the chip base; an unacceptable feature and potential cause of thermal problems.

SEM Figure 2-10 shows a wire bond to package lead frame.

2.7 WIRE BOND PULL TEST

The wire bond-pull test was performed per MIL-STD 883B, Method 2011.2 (prior to chip passivation removal). A strip chart recorder with a bond pull test setup, calibrated in grams, was used for the wire break test. The break stress for each bond is shown in Table I.

Table I. Wire Bond Pull Test in Grams

Pin No.	SN 1	SN 2	Pin No.	SN 1	SN 2
1	2.5	2.2	12	2.3	2.7
2	2.9	3.0	13	2.6	3.0
3	2.1	2.4	14	2.4	3.1
4	2.6	3.0	15	2.9	2.7
5	2.2	2.8	16	2.2	2.5
6	3.0	2.4	17	3.4	2.9
7	2.7	2.9	18	2.9	3.2
8	2.2	3.0	19	2.4	2.7
9	3.4	3.1	20	2.8	2.5
10	3.0	2.6	21	3.2	2.9
11	2.8	3.0	22	2.6	3.0

NOTE: Minimum acceptable breaking force for 1 mil aluminum wire is 2 grams.

Figure 2-8.

SEM view of die corner (SN-1) showing saw and break separation of silicon chip.

NOTE INSUFFICIENT DIE ATTACH FILLET

Figure 2-9.

SEM view of die corner (SN-2).

NOTE LACK OF DIE ATTACH FILLET

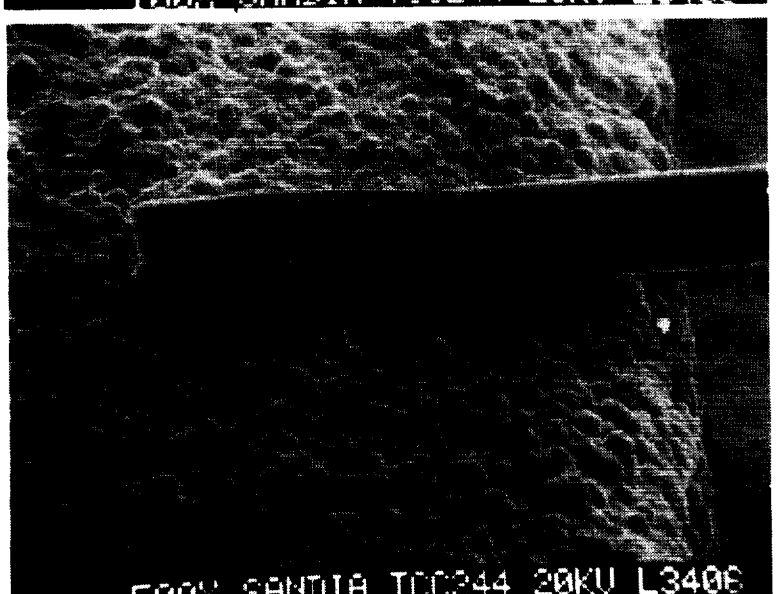


Figure 2-10.

SEM view of typical wire bond to package lead frame.

2.8 SUMMARY AND CONCLUSIONS

Package assembly and bonding integrity. The die attach and fillet in the two devices was of questionable integrity as evidenced in X-ray photo Figures 2-3 and 2-4 and SEM Figures 2-8 and 2-9, with insufficient gold eutectic fillet at the base of each chip. The die attach is assembly related and corrective steps can eliminate this type of problems.

The wire-pull bonding strength is acceptable. Optical opacity (poor transparency) of chip passivation makes the optical inspection of chip patterns difficult and inconclusive. (Also see SEM Figures 4-1 through 4-3, Section IV.)

SECTION III
ELECTRICAL DESIGN ANALYSIS

3.1 INTRODUCTION

Overall functional block diagram of the TCC 244 1K RAM chip is shown in Figure 3-1. A magnified optical photo of the chip in Figure 3-2 identifies the pads and the access functions. Correspondingly, a floor map pattern in Figure 3-3 compares with the chip's photo and identifies in detail the functional circuit blocks. Similarly, the bit logic map of the 256 x 4 memory array in Figure 3-4 is oriented to a floor map and functionally defines bit logic decoding states to the 256 x 4 array.

Figure 3-5 shows a logic diagram together with functionally equivalent detailed circuit diagram. Figure 3-6 represents the complete logic and circuit design concept.

The TCC 244, fully static asychronous CMOS RAM, is approximately comprised of 6400 active elements on silicon. Unlike a dynamic RAM, this memory does not require a refresh pulse to maintain data content validity. The definition of the RAM is that any bit location in the memory matrix can be accessed regardless of any other bit. The data may be stored (written) in the memory matrix or read out.

The physical design analysis of chip circuit cells, in terms of logic/circuit design, follows a pattern of nine circuit segments which were selected and are displayed in magnified optical photo Figures 3-7a through 3-16a, together with corresponding captions, circuit and logic diagrams.

These nine photo figures comprise and provide analytical circuit block examples which functionally represent physical design of this memory, from which the overall logic and circuit schematic have been drawn and validated.

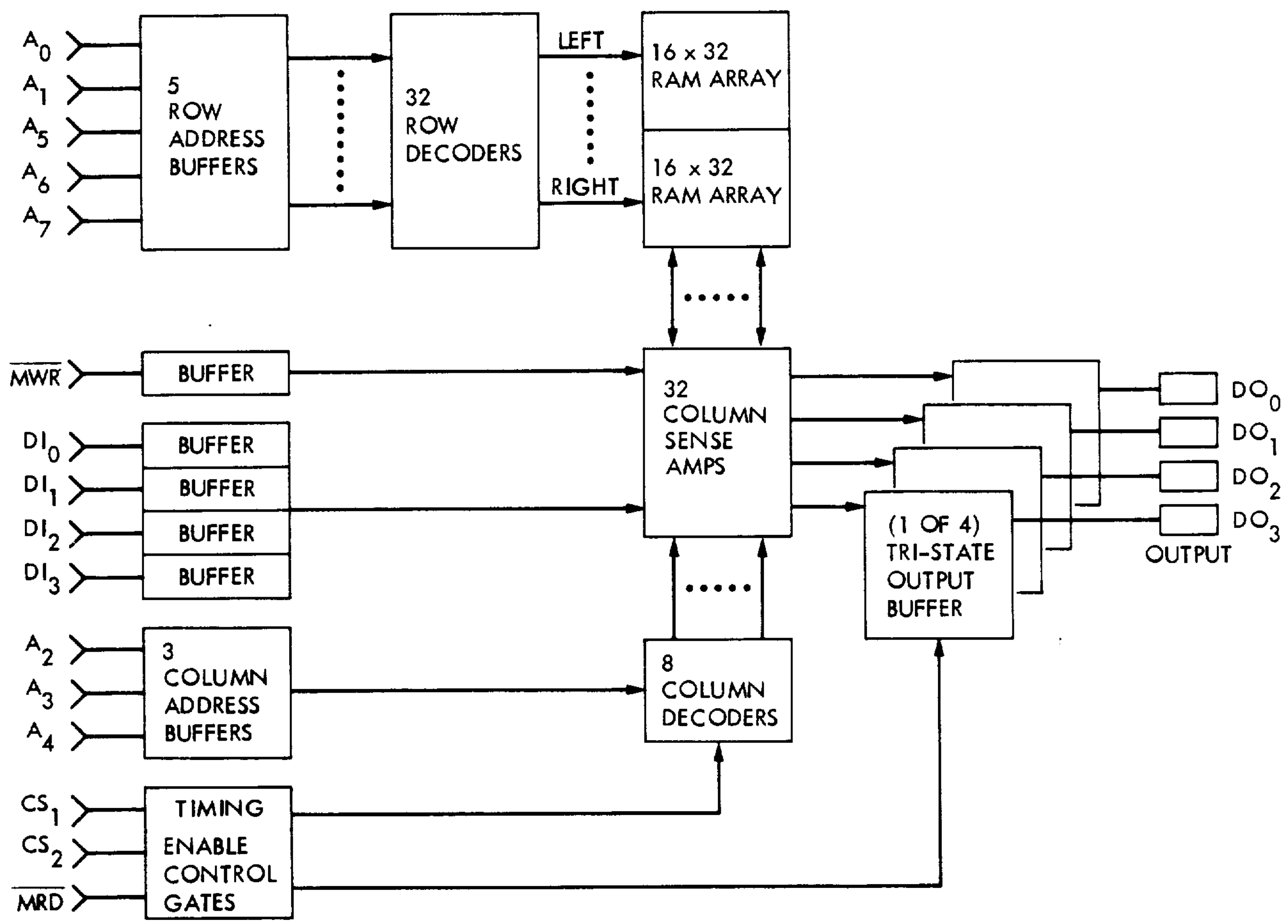


Figure 3-1. Block Diagram of TCC 244 1K CMOS RAM.

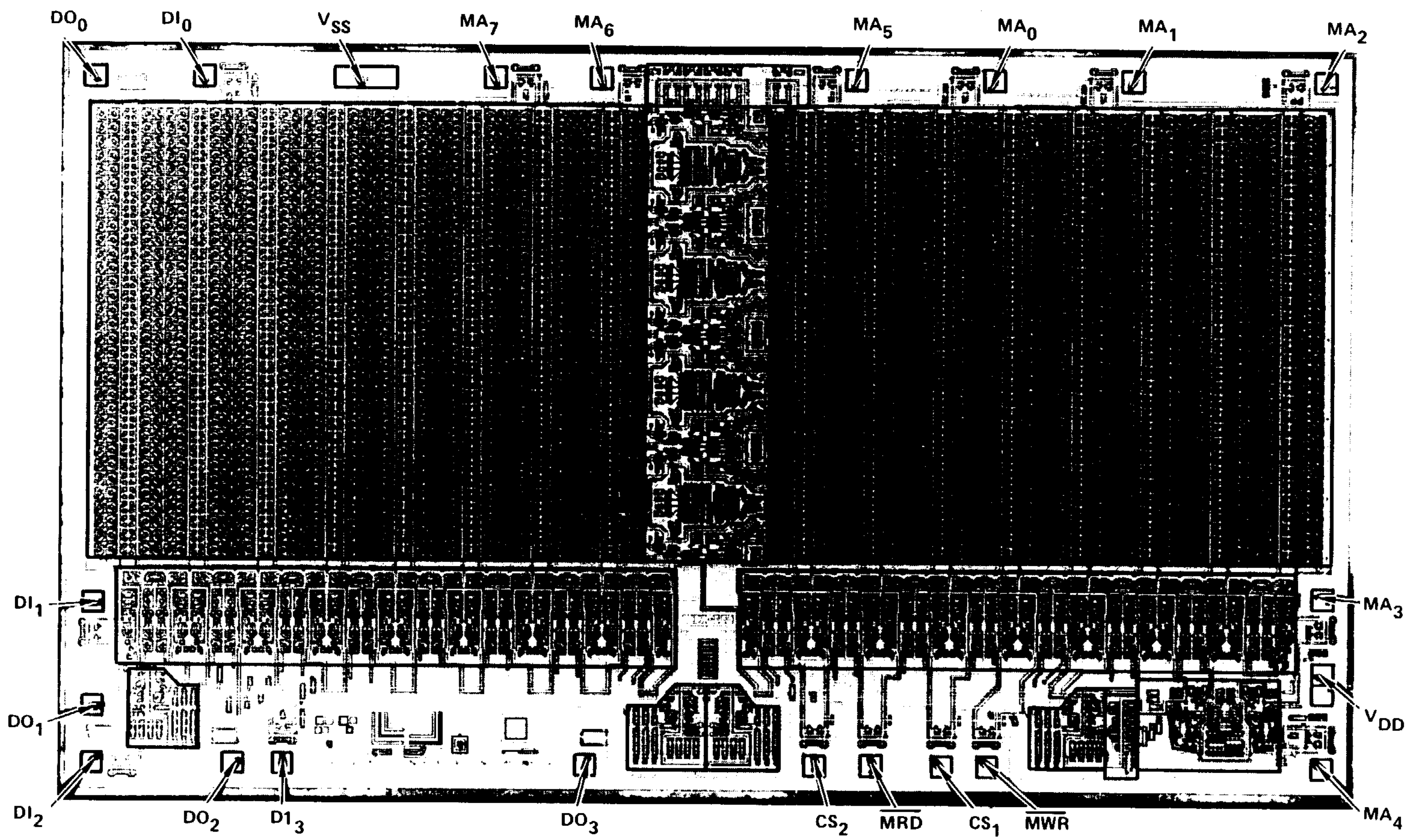


Figure 3-2. Optical view of TCC 244 1K CMOS RAM chip
(passivation removed).

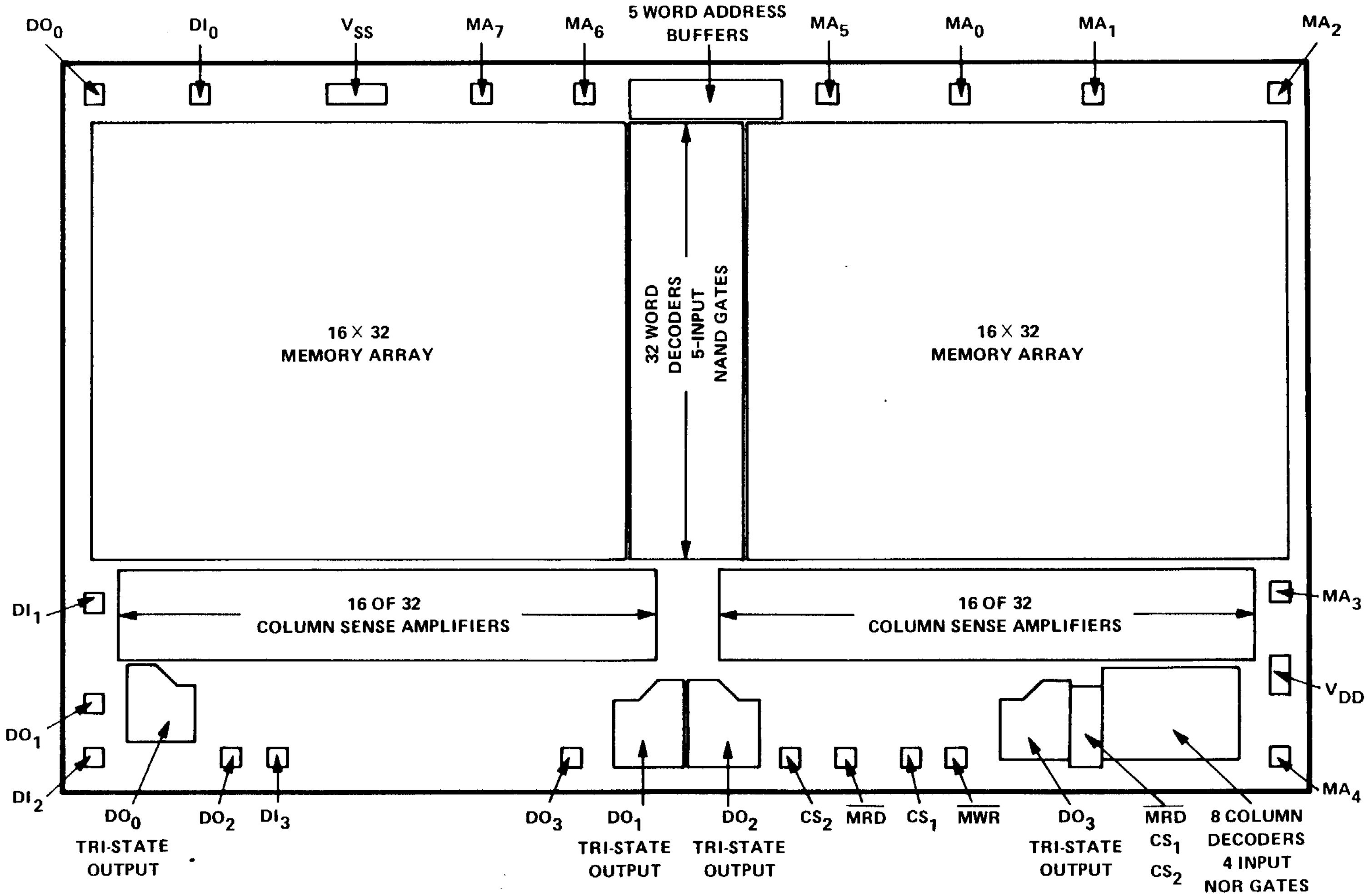


Figure 3-3. Floor map of TCC 244 1K CMOS RAM chip.

DATA φ	DATA 1	A5	A1	Aφ	A7	A6	A5	A1	Aφ	DATA 2	DATA 3
		1	0	0			0	0	1		
		0	0	0			1	0	1		
		1	0	1			1	0	0		
		0	0	1	0	0	0	0	0		
		0	1	1			0	1	0		
		1	1	1			1	1	0		
		0	1	0			1	1	1		
		1	1	0			0	1	1		
		SAME			1	0	SAME				
		SAME			1	1	SAME				
		SAME			0	1	SAME				
	1 0 0 1 1 0 0 1	A2					A2			1 0 0 1 1 0 0 1	
SAME AS DATA 1	1 1 0 0 0 0 1 1	A3					A3			1 1 0 0 0 0 1 1	SAME AS DATA 2
	1 1 1 1 0 0 0 0	A4					A4			0 0 0 0 1 1 1 1	MSB

TEST TRANSISTORS

BIT MAP FOR THE TCC 244

Figure 3-4. Bit map of the TCC 244.

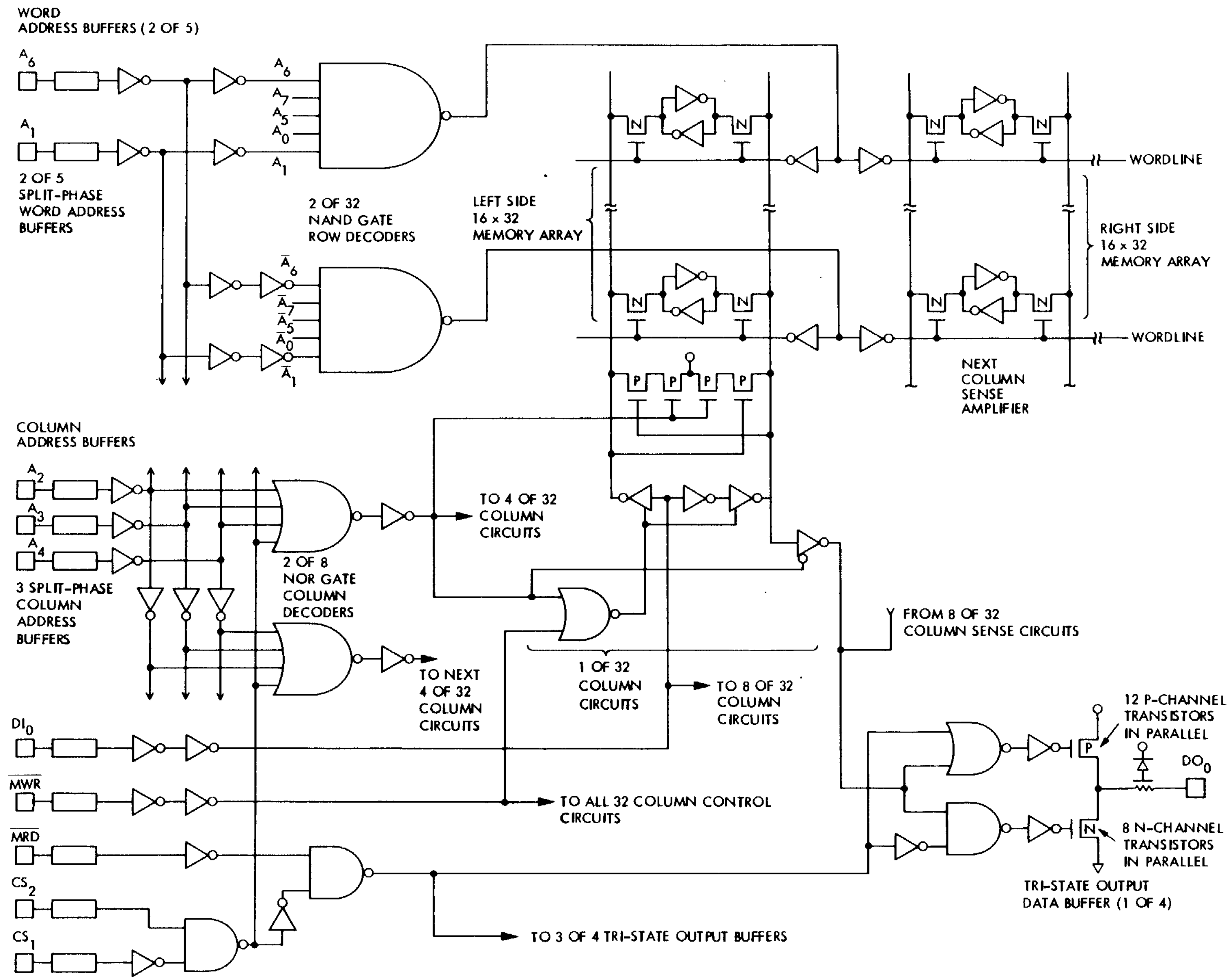


Figure 3-5. Logic diagram representing design concept of Sandia TCC 244 (256 x 4) 1K CMOS RAM.

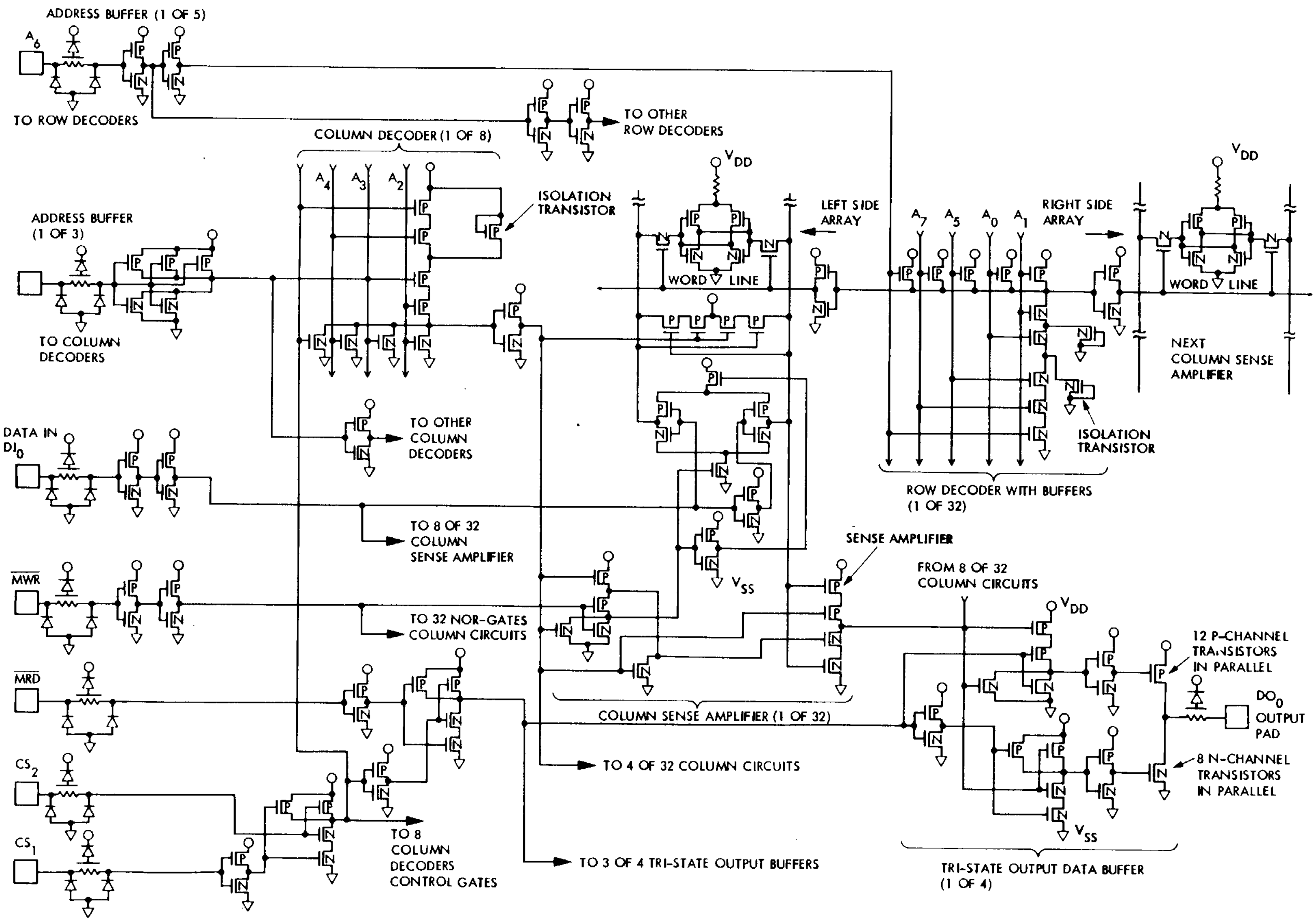


Figure 3-6. Circuit diagram of Sandia TCC 244 (256 x 4) 1K CMOS RAM.

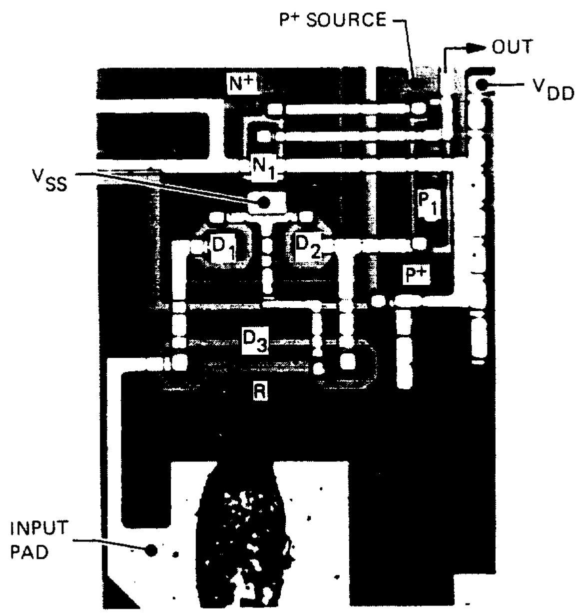


Figure 3-7a. Optical photo of data input pad (DI) and protection circuit (1 of 4).

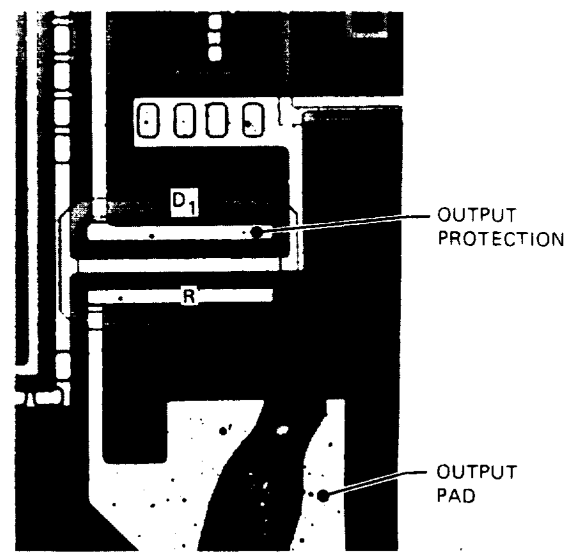


Figure 3-8a. Optical photo of output pad with protection (1 of 4).

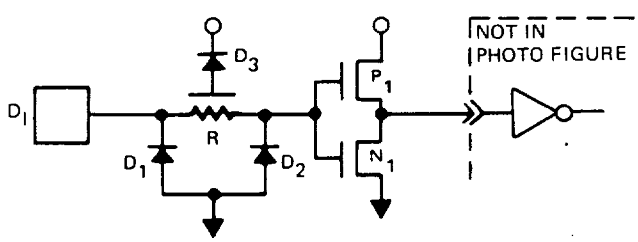


Figure 3-7b. Diagram of input protection circuit with inverter buffer.

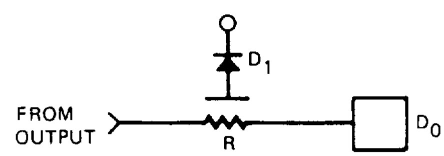


Figure 3-8b. Diagram of output protection circuit.

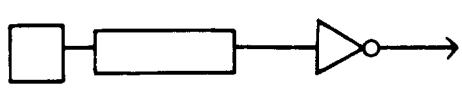


Figure 3-7c. Logic equivalent.

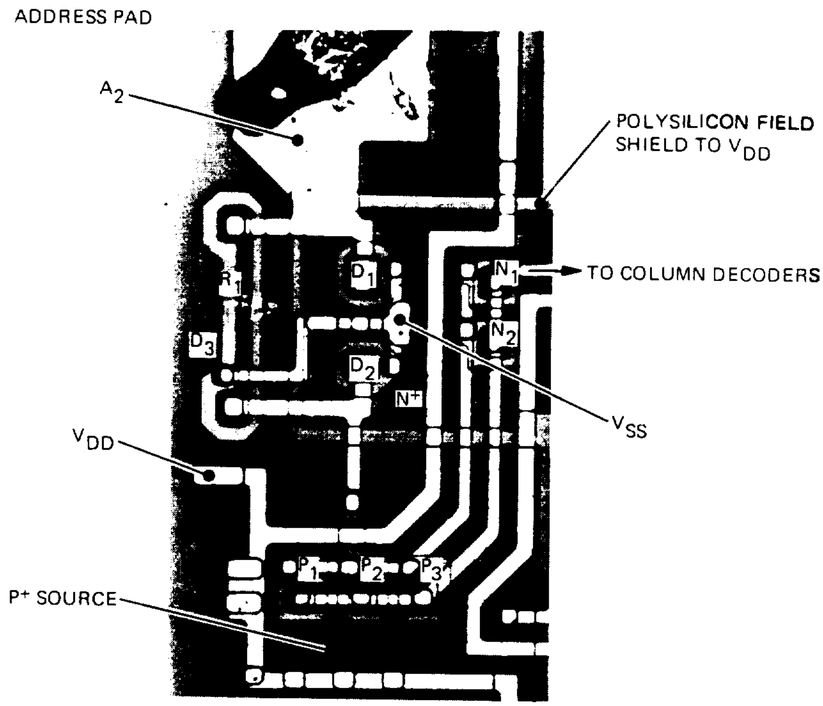


Figure 3-9a. Optical photo of data address input (1 of 3) to column decoders.

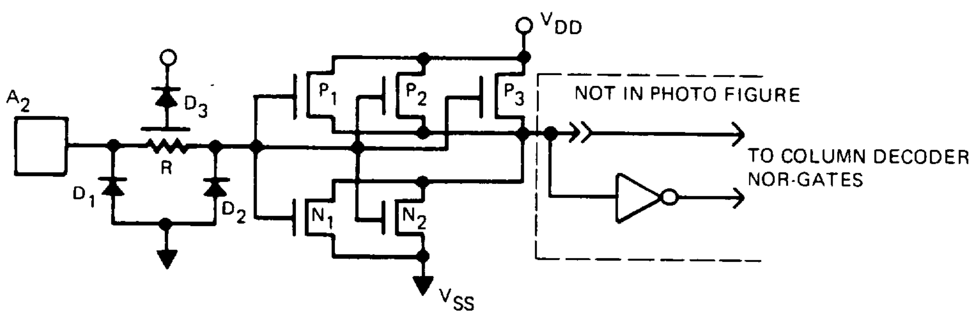


Figure 3-9b. Diagram of data address input circuit.

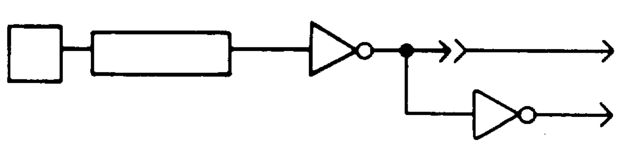


Figure 3-9c. Logic equivalent.

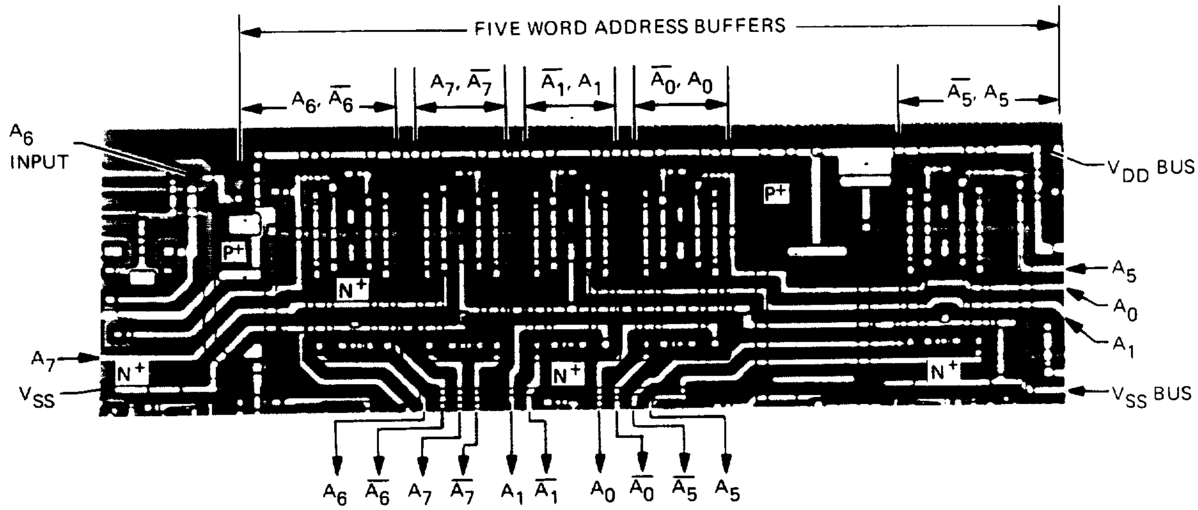


Figure 3-10a. Optical photo of 5 address buffers accessing 32 row decoders (5-input Nand gates).

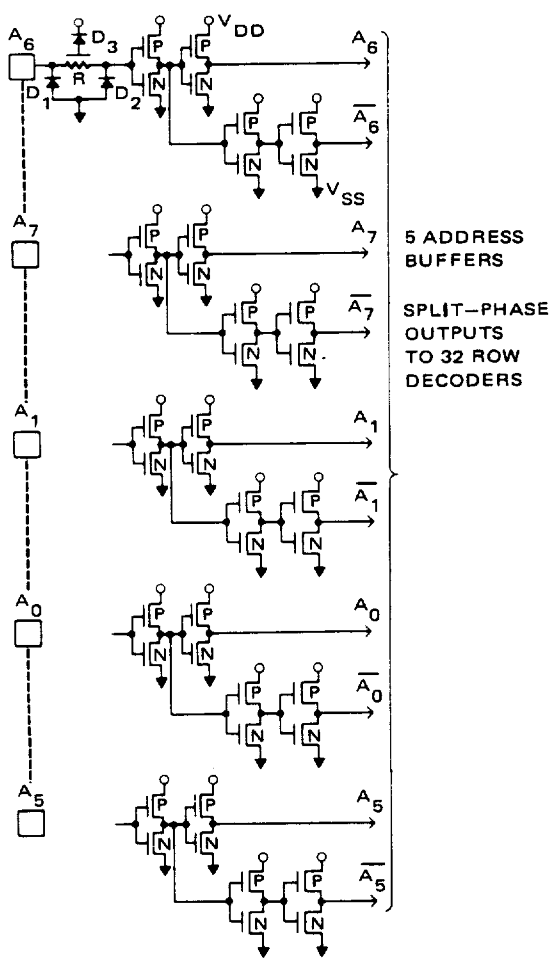


Figure 3-10b. Diagram of split phase 5-word address buffers.

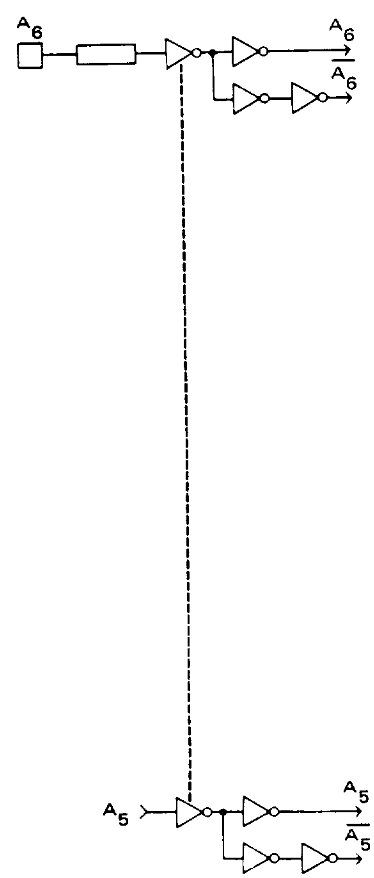


Figure 3-10c. Logic equivalent split-phase word address buffers.

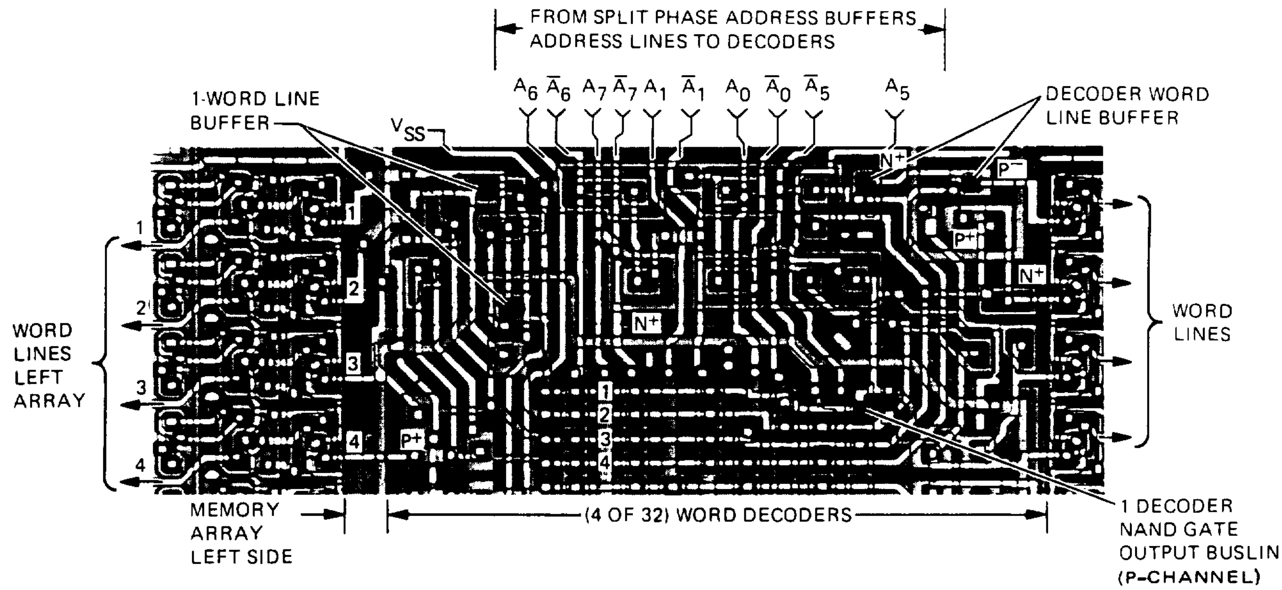
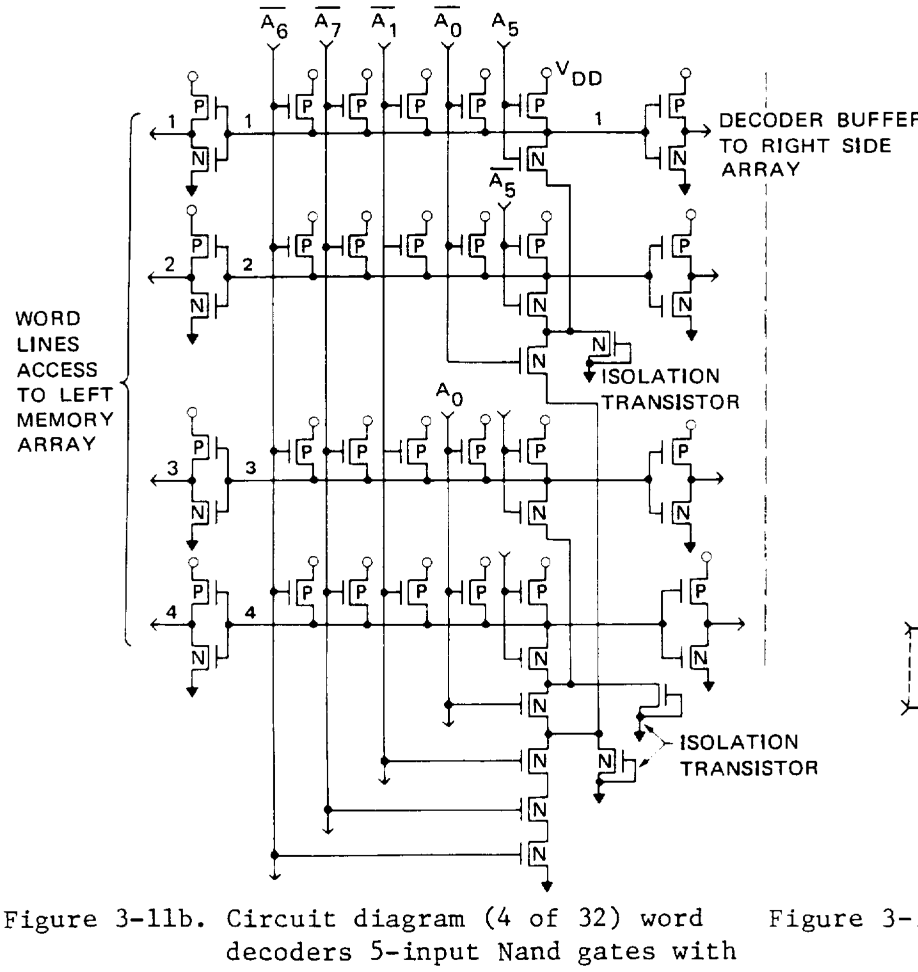


Figure 3-11a. Optical photo (4 of 32) 5-input Nand gate word decoders.



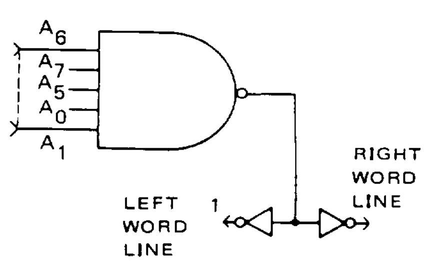


Figure 3-11b. Circuit diagram (4 of 32) word decoders 5-input Nand gates with word line buffers.

Figure 3-11c. Logic equivalent 1 of 32 word decoders.

Note: The isolation transistors (N-channel only) reduce the number of transistors for 4-word decoders by sharing N-channel series C^2L complement pattern.

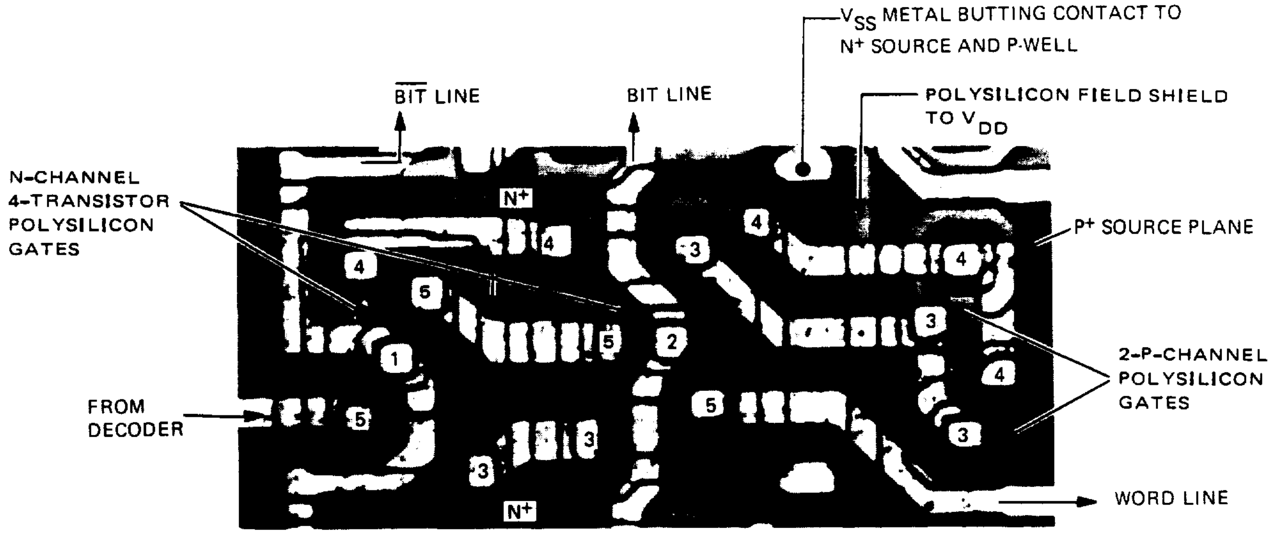


Figure 3-12a. Optical photo of C^2L CMOS 6T memory cell.

Note: The numbered interconnect nodes of 6-transistors are cross-identified with circuit diagram.

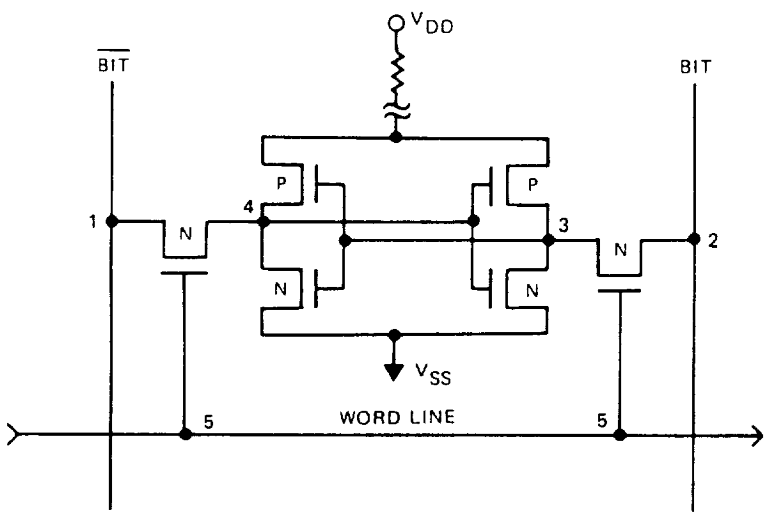


Figure 3-12b. Diagram of 6-transistor CMOS memory latch.

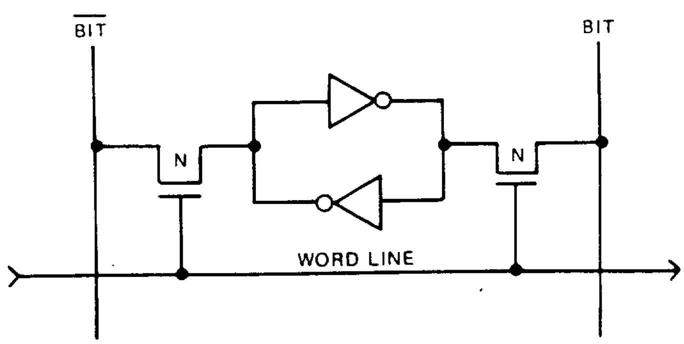


Figure 3-12c. Logic equivalent.

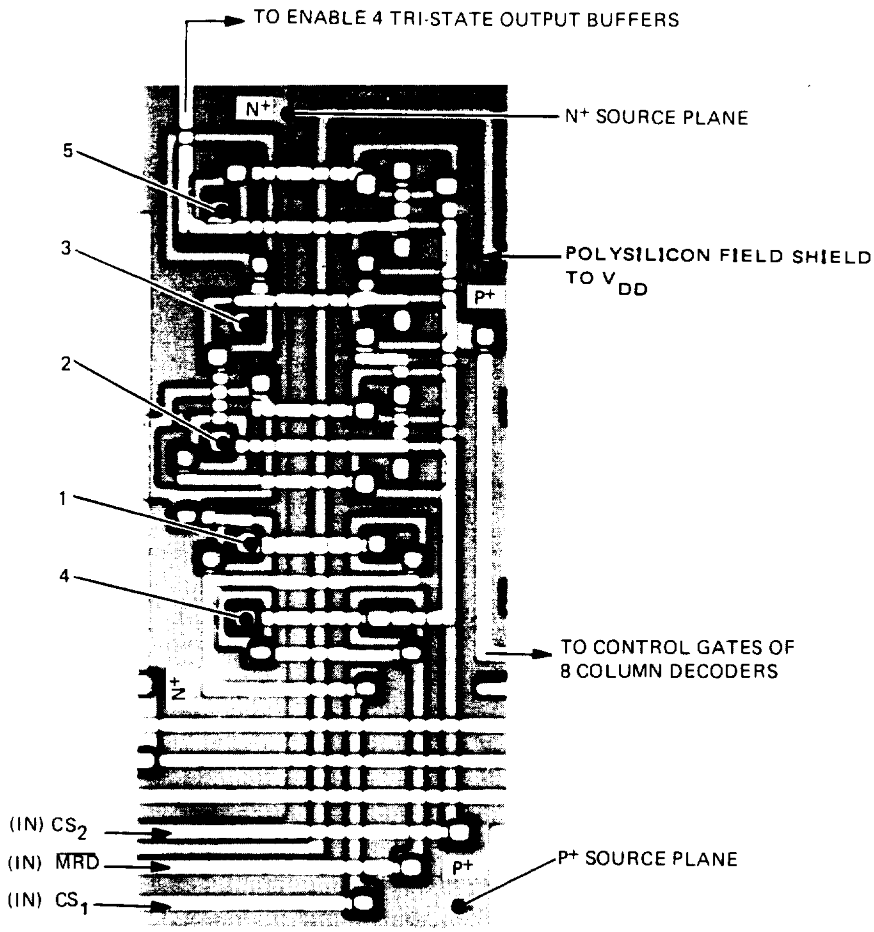


Figure 3-13a. Optical photo of control gates CS_1, CS_2 and $\overline{MRD}$.

Note: The identifying numbers in photo figure are cross-referenced with circuit node-numbers.

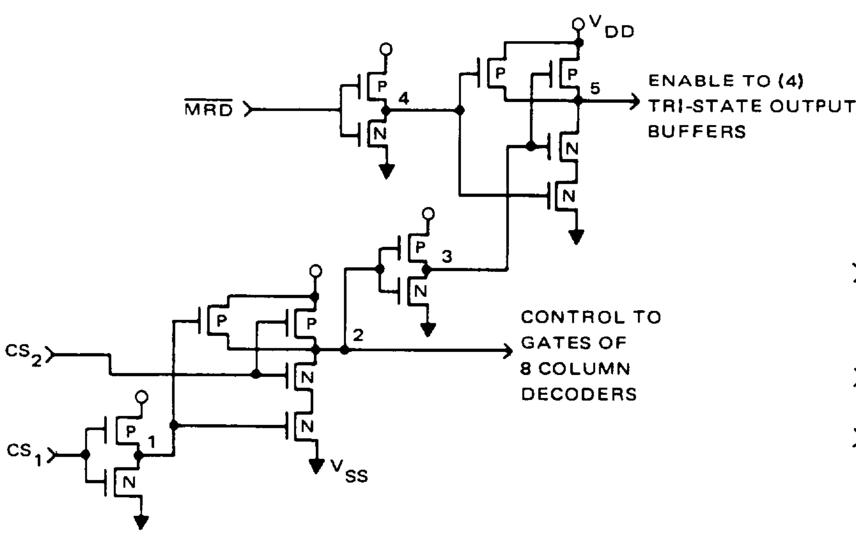


Figure 3-13b. Circuit diagram of control gates/buffers CS_1, CS_2 and $\overline{MRD}$.

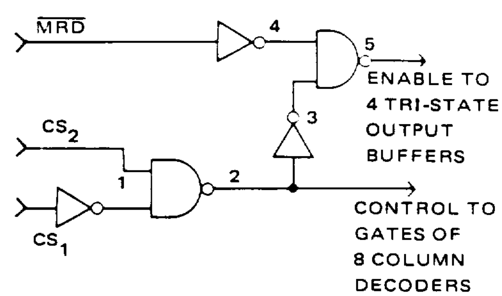


Figure 3-13c. Logic equivalent.

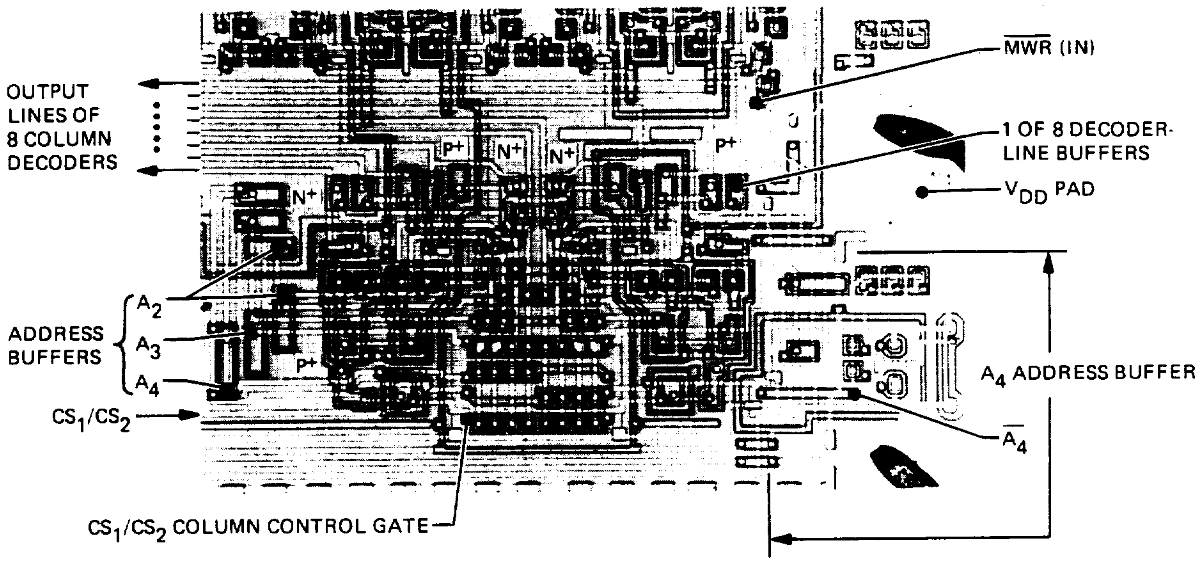
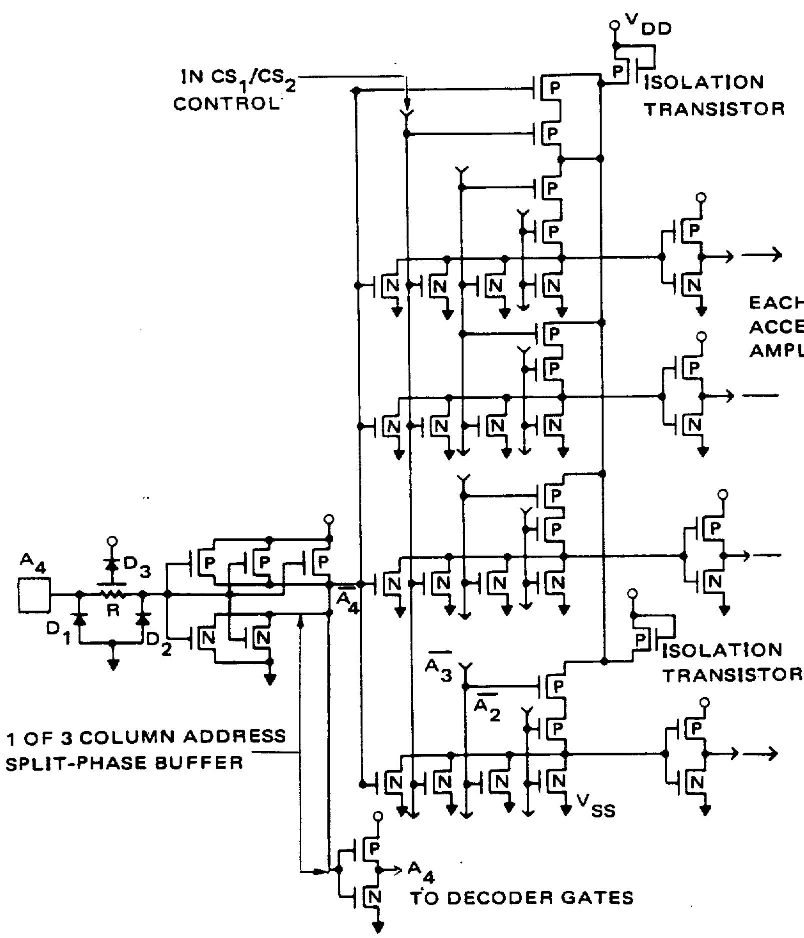


Figure 3-14a. Optical photo of 8 column decoders 4-input Nor-gates with buffers.



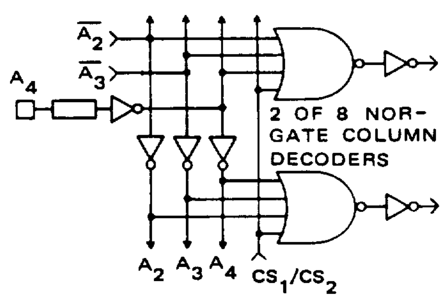


Figure 3-14b. Circuit diagram (4 of 8) decoders 4-input Nor-gates with buffers.

Figure 3-14c. Logic equivalent.

Note: The isolation transistors (P-channel only) reduce the number of P-channel transistors for 4 decoders by sharing P-channel series C^2L complement pattern.

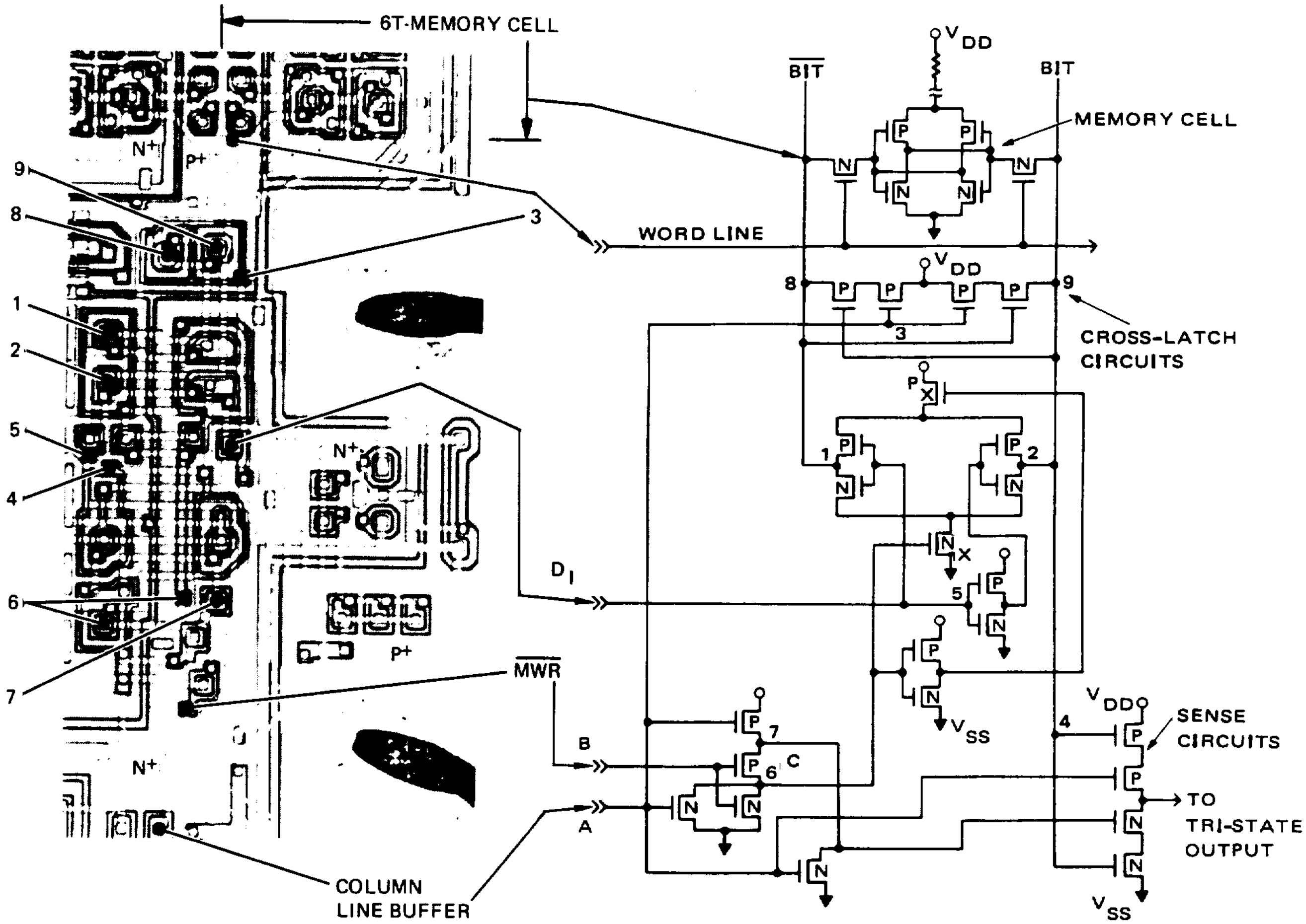


Figure 3-15a. Optical photo of complete 1 of 32 column sense/switching amplifier from column line buffer (bottom) to 6T memory latch, top.

Note: The identifying numbers in photo figure are cross-referenced with circuit-node numbers.

Figure 3-15b. Circuit diagram (1 of 32) column sense amplifiers.

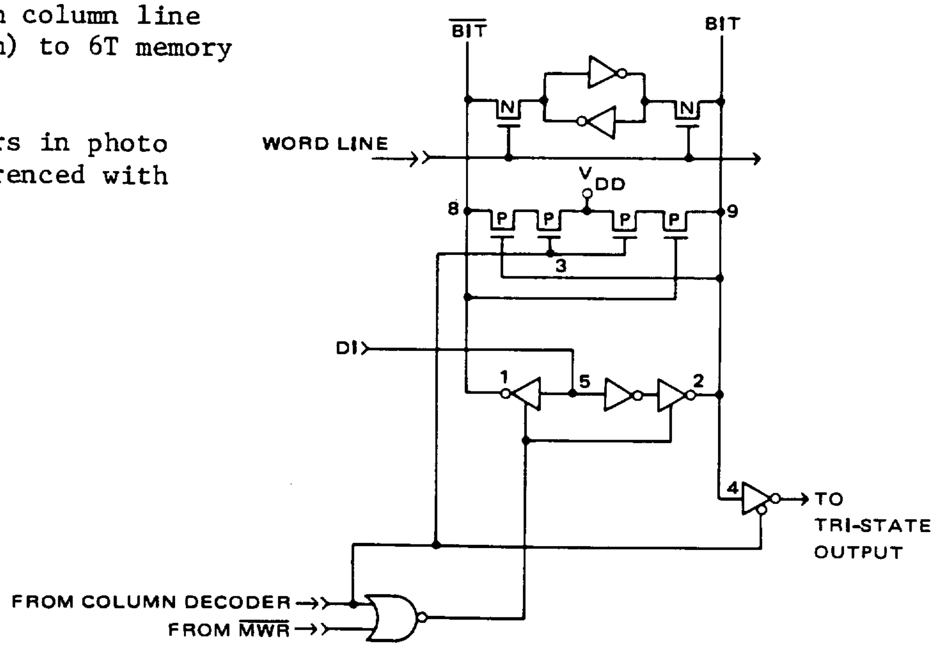


Figure 3-15c. Logic equivalent.

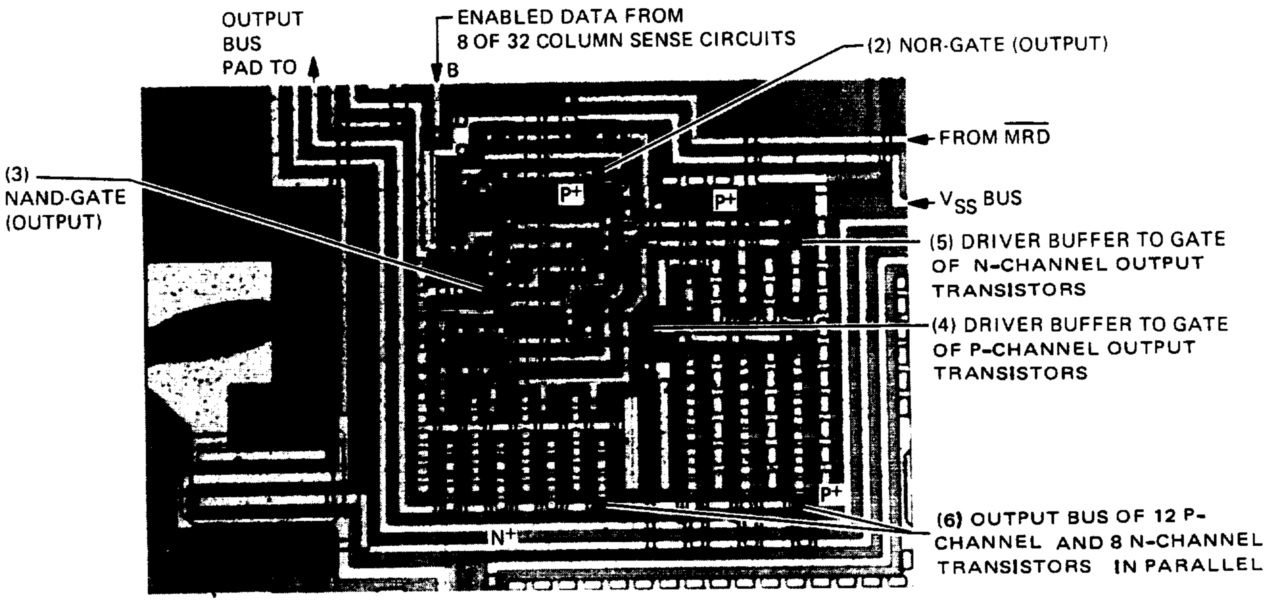


Figure 3-16a. Optical photo of tri-state data output buffer (1 of 4).

Note: The identifying numbers in photo figure are cross-referenced with circuit node numbers.

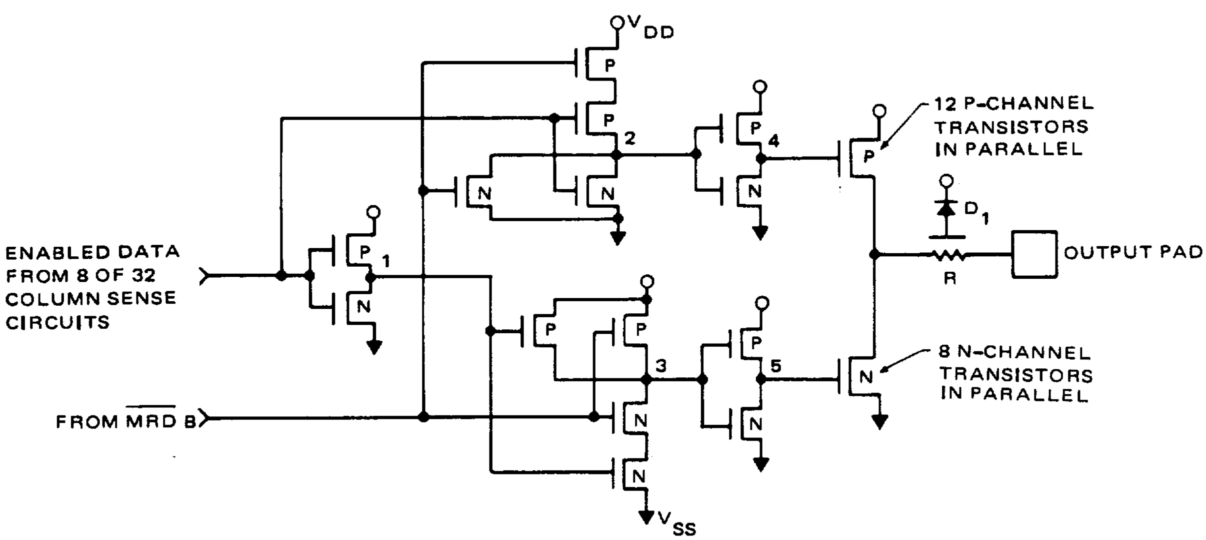


Figure 3-16b. Diagram of tri-state output buffer circuit (1 of 4).

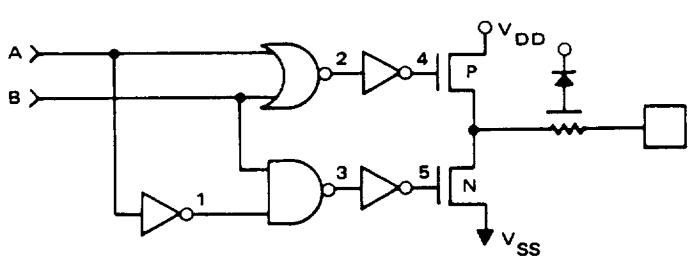


Figure 3-16c. Logic equivalent.

3.2 DESIGN PATTERN AND FUNCTION

The TCC 244, 256 x 4 bit RAM design utilizes four types of logic cells, (e.g., inverter Nand-gates, Nor-gates, 6-transistor bistable memory latches and tri-state-gate output buffers with pull-up pull-down P-channel and N-channel output configuration with a protection. All of the input functions on the chip are protected with a resistor and protection diodes, Figure 3-7a.

3.3 READ MODE

With $\overline{MWR}$ high, the addressed binary data in a 256 x 4 memory array is accessed from eight data address buffers (A_0 - A_7), each comprised of four inverting buffers with split-phase (A, $\overline{A}$) dual outputs (Figures 3-5, 3-10a and 3-10b).

Five of the eight address buffers; A_0, A_1, A_5, A_6 and A_7 with $\overline{A}$ complements access the memory through thirty-two word-decoders, 5-input Nand-gates with inverter-buffered outputs, in 4 blocks of 8 decoders. From the chip center, each word decoder output drives one left side word line to 32 N-channel pass-transistor gates and right side word line to 32 N-channel pass-transistor gates. (Figures 3-5, 3-11a and 3-11b.) Note: Only address data buffers access the 32 word decoders with no other enable/disable function lines.

Three of the eight address buffers A_2, A_3 and A_4 with $\overline{A}$ complement access the memory array through eight column decoders four-input Nor-gates with inverter-buffered outputs. Each column decoder accesses one column sense amplifier and a P-chan cross-latch circuit in each 4 blocks of 8 column sense amplifier circuits.

The function of a P-channel 4-transistor cross-latch circuit in each column sense amplifier circuit is to help the 32 memory cells in that column in steering the internal sensed data on (bit, $\overline{\text{bit}}$) lines of pass-transistor outputs. (Figure 3-6, 3-14b, and 3-15b.)

With $\overline{MWR}$ high in read-mode, the eight column decoders, when enabled by CS_1 and CS_2 control gates, together with an appropriate data address pulse on each decoder, access the 32 column sense circuits which sense the data at (bit, $\overline{bit}$) sense lines in 4 blocks of 256 memory cells when they are appropriately cross-addressed through 32 word lines of word decoders, and are subsequently enabled by $\overline{MRD}$, CS_1 and CS_2 control gates (Figure 3-13b) to the four corresponding tri-state data output buffers DO_0 - DO_3 and displayed at the output pads. (Figures 3-5, 3-6, 3-15b and 3-16b.)

3.4 WRITE MODE

In the write cycle the programming binary data enters four data input buffers DI_0 - DI_3 (Figures 3-5, 3-6 and 3-7). Each of the four data input buffers provides a data path with parallel input interface to 8 column sense amplifier circuits in 4 blocks of 8 amplifiers. (Figures 3-5, 3-6 and 3-16b.) Consequently, each block of 8 column sense circuits with 8 pairs of (bit, $\overline{bit}$) sense lines accesses and controls a block of 256 memory cells. The program sequence of written data with each 4 blocks of 256 memory cells is determined by the logic address of 8 address buffers, A_0 - A_7, and the corresponding word and column decoders selecting the memory cells in the 256 x 4 bit array.

An illustrated example of one column sense amplifier circuits cells are identified in Figure 3-15b and their functions in write and read cycles described: in write cycle when $\overline{MWR}$ is low the selected column points A and B are driven low, the output of Nor-gate point C is high causing P_x and N_x transistors to be turned on and the input data and data (bit,$\overline{bit}$) lines are divided to override previous bit content in the cell, and with word select enabling the data bit on the line to be written in the selected cell.

In read cycle with $\overline{MWR}$ high the column is selected, points A and B will be low and high, respectively, and point C will be low, N_x and P_x transistors will be off with the data line being isolated from the sense circuit.

3.5 SUMMARY OF ELECTRICAL DESIGN PATTERNS AND CONCLUSIONS

The physical design of this 1K CMOS asynchronous RAM chip, because of complementary P^+ and N^+ source plane patterns and relatively large (C^2L) closed polysi-gates, presents easily recognizable symmetry of laid out circuit blocks.

NOTE: Minimal materials process description in terms of this circuit function is partially included as part of the Electrical Design Summary.

Both decoding circuits, the 32-word decoder Nand-gates and 8-column decoder Nor-gates, in their series-transistor-cell complements of each Nand-gate N-channel, and Nor-gate P-channel, use in the design a lesser number of P or N transistors compared to their parallel complement in each block of four gates (Figures 3-11a, 3-11b, 3-14a and 3-14b). The gate design, sharing approach of a series transistors complement for Nand-gates and Nor-gates helps to reduce physical area and the chip size, and the logic gates still meet functional requirements.

In order to implement this design for (C^2L) circular polysi-gate pattern and in isolating a common source plane, two or three additional isolation transistors are used for a functional block of four gates (see the above figures).

The interconnect of word line bus consist of multiple metal to polysi-gate links. Each six-transistor memory latch of the matrix contains 16 contacts, compared to patterns of 6-T cells of other CMOS technologies having memory latches with 8 to 10 contacts. With the increased number of contacts, the R/C value as a delay function equally increases.

In the design of each memory column with 32 cells, the electrical path for 64 P-channel transistors P^+ source plane has at both ends, a very narrow P^+ diffusion path (defined by a P^+ diffusion mask step). These paths are then terminated to a V_{DD} bus (Figure 4-38, Section IV, identifies P^+ pattern).

There is no evidence of other butting contacts from each P^+ source plane to N-substrate and V_{DD}. This configuration likely reduces the current paths for P-channel transistors in each column.

However, the main reliability considerations appear to remain in the interface of all polysi patterns (e.g., gates, field-shields and polysi-gated input resistors and diodes). From physical evaluation, it appears that all of these polysi gate patterns together with their contacts interface terminations rest entirely on top of thin gate-oxide, even in the insulating separation between V_{DD} and V_{SS} buses.

Though, this may be acceptable, the layout in this (C^2L) CMOS polysi pattern interface does not seem to show typical design rule practice (see Figures 4-31 and 4-32, Section IV). In most LSI/VLSI CMOS designs polysi contact interface terminations are usually extended and placed on the thicker field oxide part.

Because of all of the polysi interface and the insulating separation from silicon substrate is with thin gate-oxide only; the entire design of this memory places a heavy functional dependence on its insulating quality and its reliability of the long term use of the device. Because of the thin oxide insulating function, the potential areas of precipitating breakdowns would also appear to be beneath the polysi-gate-areas in the metal contact interface and the vertical proximity of polysi thickness interfacing with thin oxide in channel paths.

In a follow-up, the cause for this concern may reside in the effect of a metal sintering step of the metal interconnect for preferential surface alloying of aluminum with polysi and silicon contacts for a good interface. (The sintering step is a time and temperature dependent function, and generates a certain stress and materials change at silicon interface.)

The gate oxide together with contact patterns in polysi over channel paths are potentially latent areas of possible and random oxide breakdowns in any place on the chip, and may affect its reliability. The thin-oxide breakdown integrity needs to be electrically evaluated with greater attention because of these conditions in materials interface, before this device is considered for high-reliability systems use.

SECTION IV

TCC 244 CHIP MATERIALS EVALUATION

4.1 APPROACH

Physical materials analysis was performed in four steps, chemically removing each layer of surface material on the chip (wet chemical etch), to reveal subsequent levels of materials with minimal structural degradations.

At each step, the exposed level of chip materials was examined optically and with a Scanning Electron Microscope (SEM). X-ray spectroscopy was also utilized for materials identification and contaminants. The visual evidence, presented in the optical and SEM photo Figures 4-1 through 4-39 together with detailed captions and comparisons provided thereby, offers insight into the exposed materials and design structures.

The four etching steps are correlated with Figures in Table II.

The emphasis at each level of materials exposure and through the SEM figures is to visually establish comparisons of these materials and in the replicating patterns after these materials that have been removed, as well as in the definition of process anomalies and ultimately in a reliable assessment of chip materials patterns.

NOTE: However carefully the multiple etching steps are performed in the removal of chips materials, the effect of lateral etch cannot be avoided; it can, however, be controlled, minimized and fully explained.

4.1.1 SEM EXAMINATION PRIOR TO TOP PASSIVATION REMOVAL

SEM inspection of the chip SiO_2 passivation reveals fine and uniform granular texture over field oxide and polysi gates, but shows minimal granularity over the chip metal interconnect. Passivated contact interface of interconnect can be identified beneath the passivation coverage. SEM Figure 4-1 displays SiO_2 passivated chip segment of A_6 address pad and input protection and address buffer with a section of word decoder and 10 memory cells. SEM Figures 4-2 and 4-3 show magnified segments of the above figures, the SiO_2 passivation morphology is clearly defined. Subsequently the passivation on the entire chip was examined for pinholes, contamination and other anomalies.

Table II. Four-Step Wet Chemical Etch Materials Removal on the Chip

Step	Description
1	Top SiO_2 passivation removed; Aluminum metallization exposed. (SEM Figures 4-4 thorugh 4-17.)
2	Aluminum metallization removed; interlevel insulating SiO_2 exposed with contact apertures to polysi and silicon diffusions. (SEM Figures 4-19 through 4-26.)
3	Interlevel insulating SiO_2 removed; exposed polysi gates. (SEM Figures 4-28 through 4-37.)
4	Polysi gates and thin oxide removed; exposed P^+ and N^+ silicon diffusions in substrate. (SEM Figures 38 and 39.)

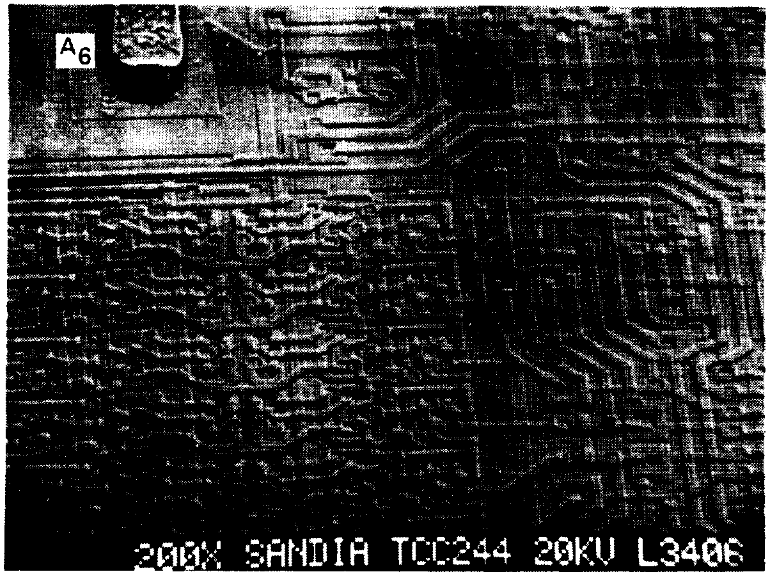


Figure 4-1.

SEM view of passivated chip segment area of A_6 data address, memory matrix and row decoder segment.

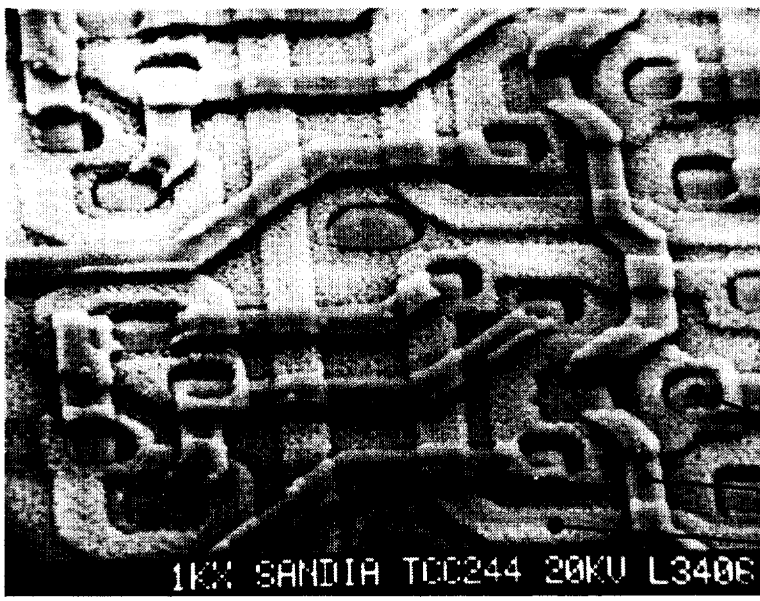


Figure 4-2.

Magnified SEM view of oxide passivation over metal interconnect and polysi (ref. Fig. 4-1) memory matrix.

Note fine granularity of passivation over polysi pattern and field oxide.

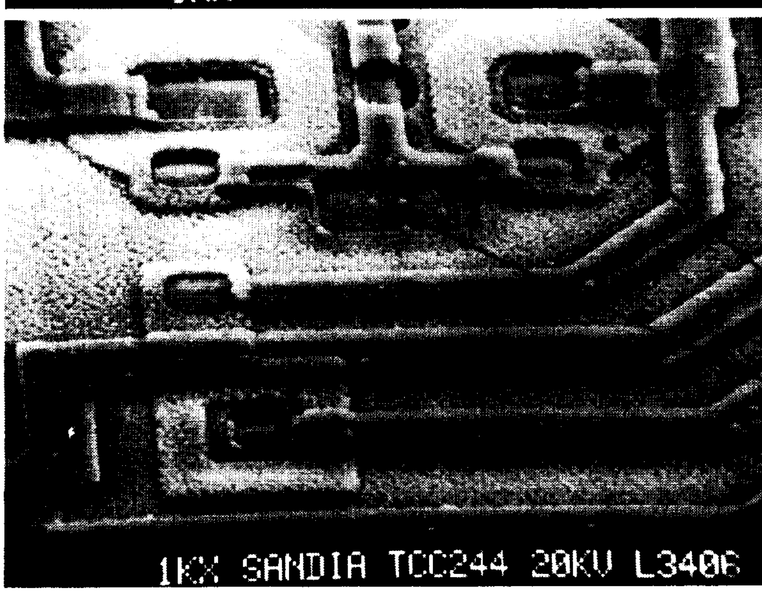


Figure 4-3.

Magnified SEM view of passivated, two input (polysi-gated) protection diodes and contacts.

4.2 STEP 1: SEM EXAMINATION AFTER TOP PASSIVATION REMOVAL

The protective passivation was removed from the chip surface to expose, intact, the metallization interconnect, and the interlevel insulating SiO_2 which still covers and separates the polysi-gates from top metal level.

The chip metallization interconnect was subsequently examined, optically and in the SEM, for metal step coverage over oxide and polysi steps, and contact interface to polysi and silicon diffusions.

SEM Figures 4-4 through 4-17, together with descriptive captions, identify and present in various positions and magnifications, certain circuit segments with the exposed metallization; showing typical examples of metal line widths, step coverage and thickness over oxide insulated polysi-gates and field shields, and other examples of metal contact interface to polysi-gates and silicon diffusions.

The metal patterns displayed in these segments represent the average metal interconnect quality of the two examined TCC 244 chips.

4.2.1 SUMMARY

SEM Figures 4-1, 4-12 and 4-14; all with magnified contact interface to polysi gates, show the worst case examples but of acceptable metal step coverage over oxide steps to polysi contacts with approximate metal thickness at the step.

Magnified aperture perimeters of contacts in interlevel oxide define the approximate thickness of insulation and the contact area interface of polysi gate SEM Figures 4-11 and 4-14. Another feature is in a large number of contacts; for example, a six transistor memory cell (Figure 4-21) has 16 contacts not including V_{CC} and V_{SS} bus compared to other CMOS technologies and 6-T memory cells which have 8 or 10 contacts.

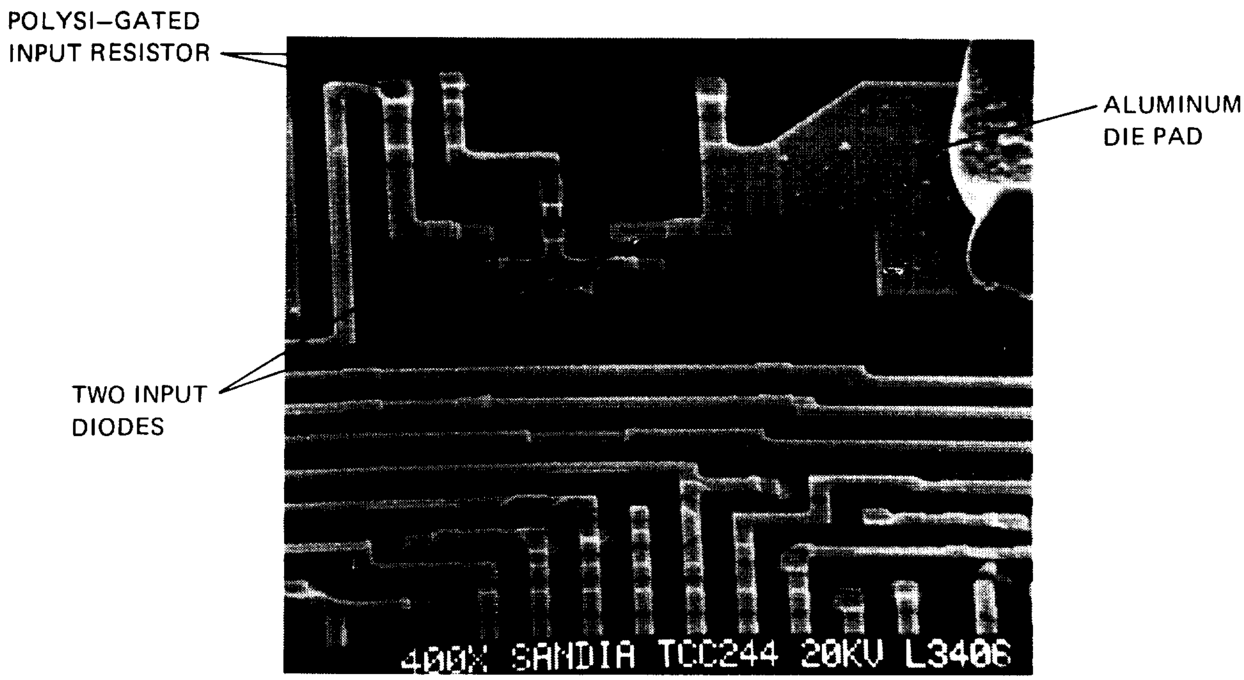


Figure 4-4. (Passivation removed) SEM view of input protection, two polysi-gated diodes and a resistor with metal interconnect.

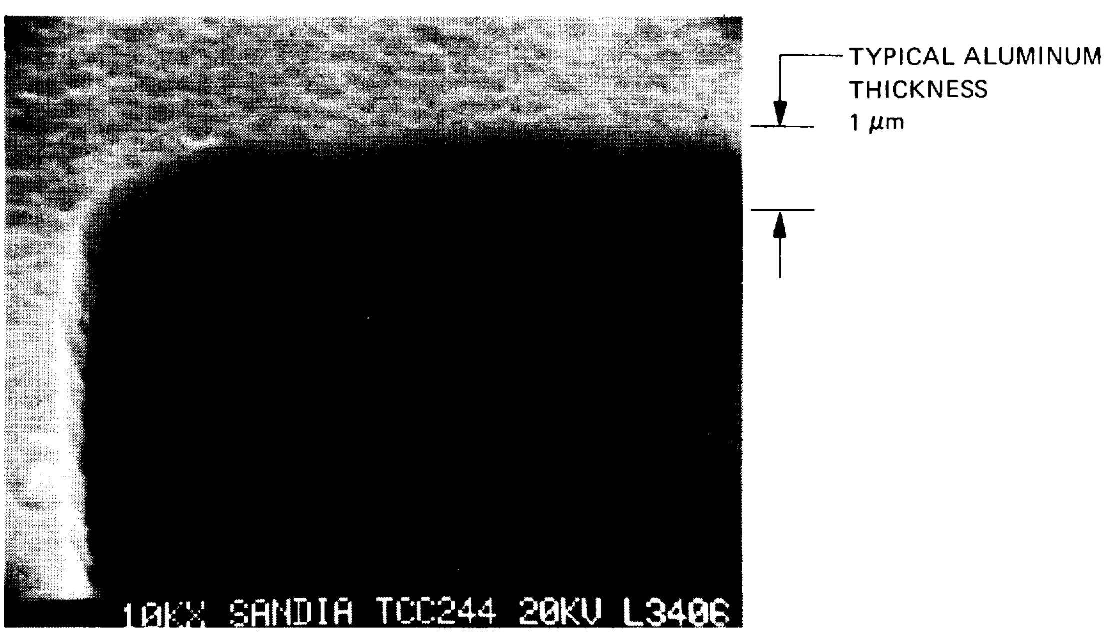


Figure 4-5. 10,000x magnified SEM side view at 70° tilt of metallization thickness.

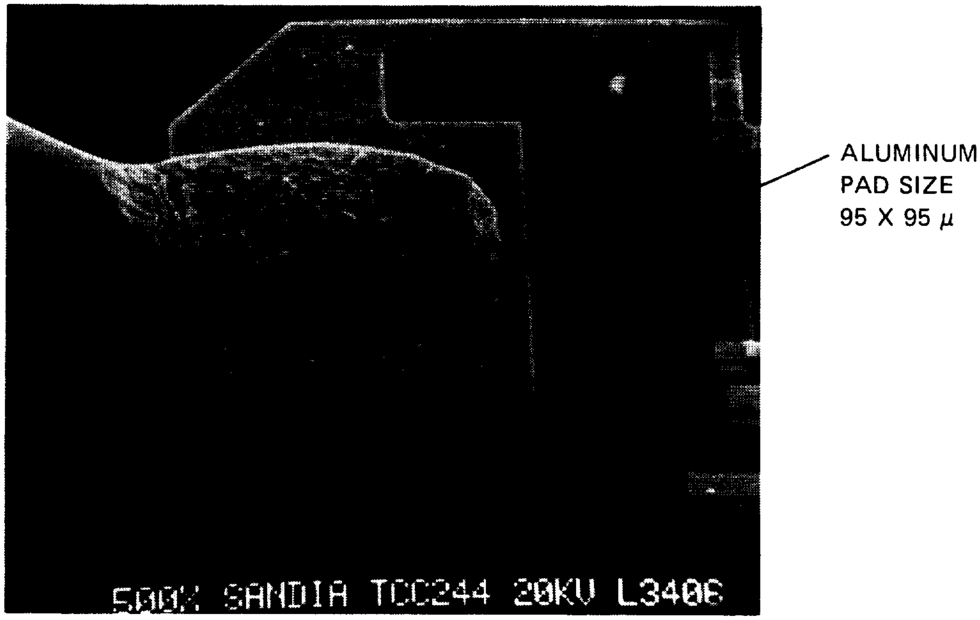


Figure 4-6. 500x SEM view of exposed metal pad with a typical wire bond.

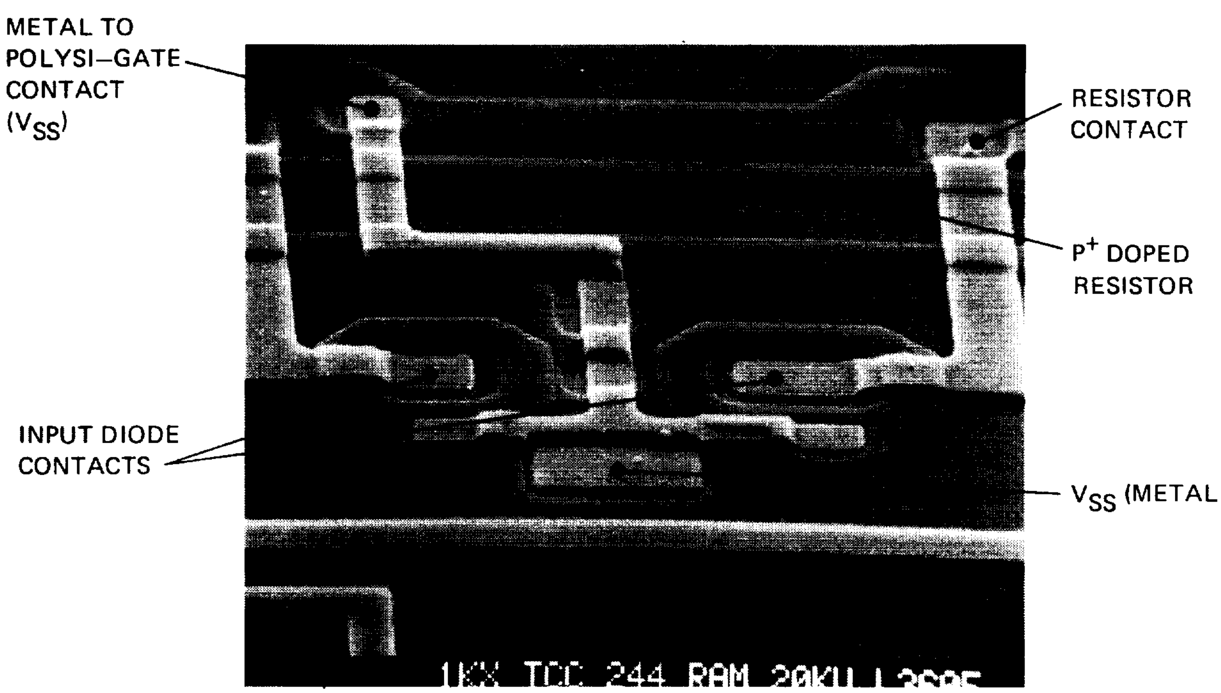


Figure 4-7. (Passivation removed.) 500x SEM view of input protection gated-resistor and two gated diodes.

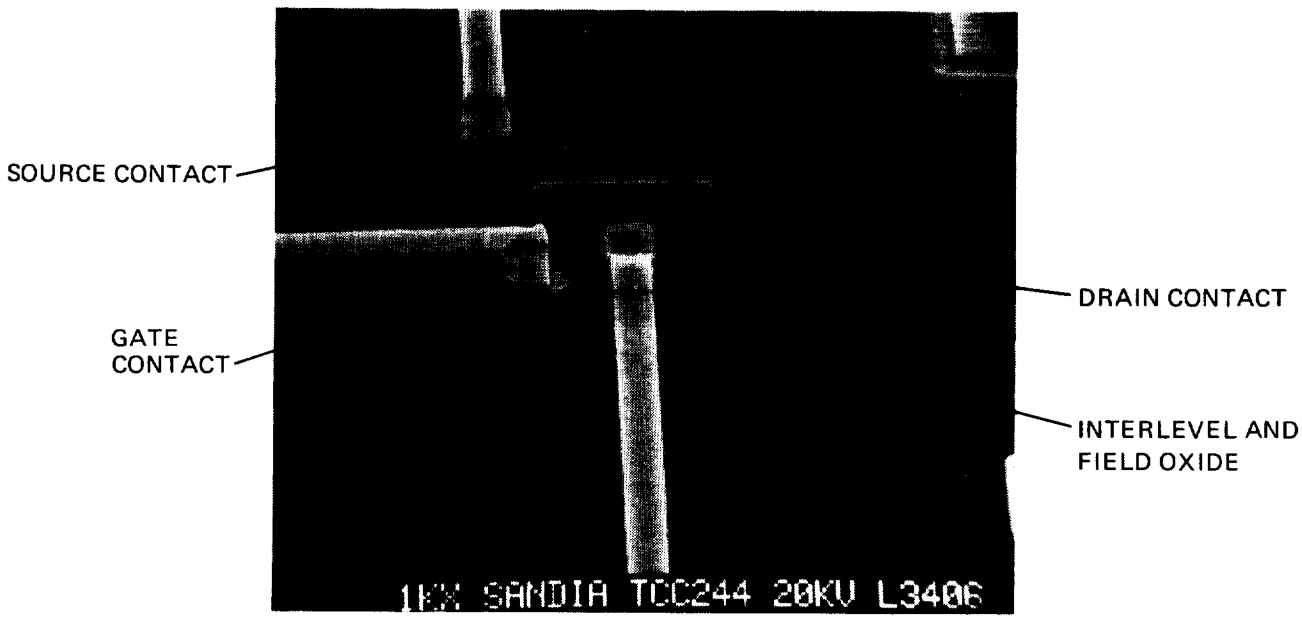


Figure 4-8. (Passivation removed.) SEM view of P-channel FET (C^2L) test transistor with interconnect.

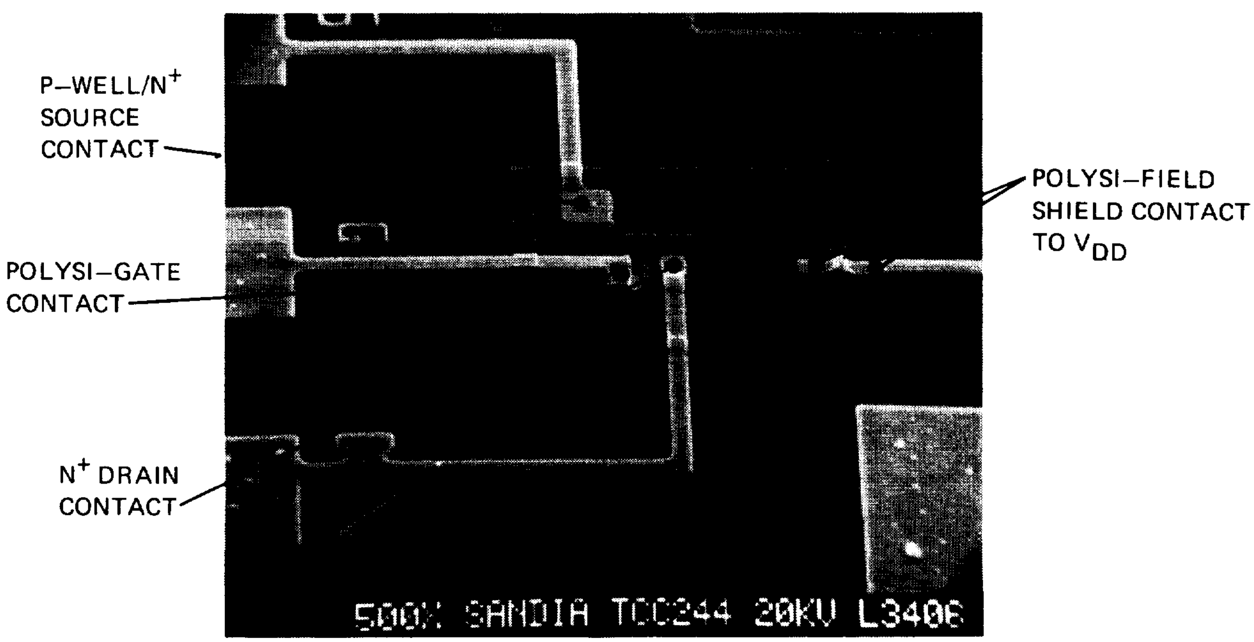


Figure 4-9. (Passivation removed.) SEM view of N-channel FET (C^2L) test transistor with interconnect. Note outer rectangular polysi-gate is a field-shield surrounding a P-well with N^+ region tied to V_{DD}.

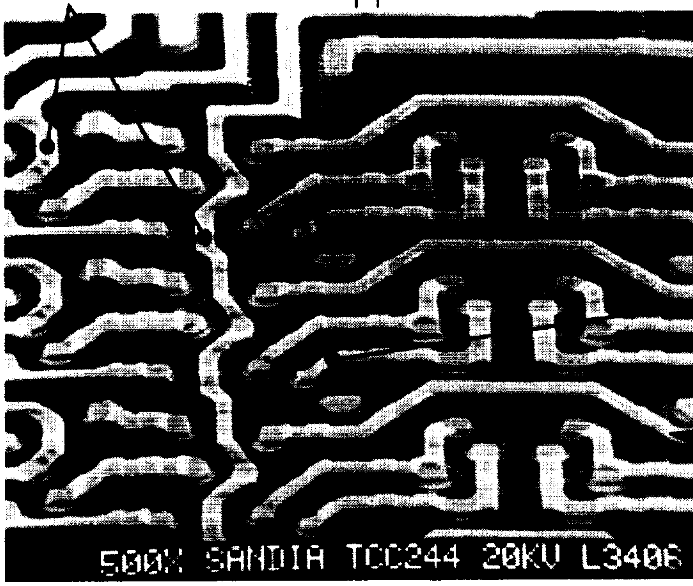


Figure 4-10. (Passivation removed.) SEM view segment of memory array with three 6-transistors memory cells and metal interconnect.

Figure 4-11. 5000x magnified SEM view of metal step over oxide to polysi-gate contact.

Figure 4-12. 5000x SEM view of metal step coverage over oxide and polysi gate. (Ref. Fig. 4-10, B contact.)

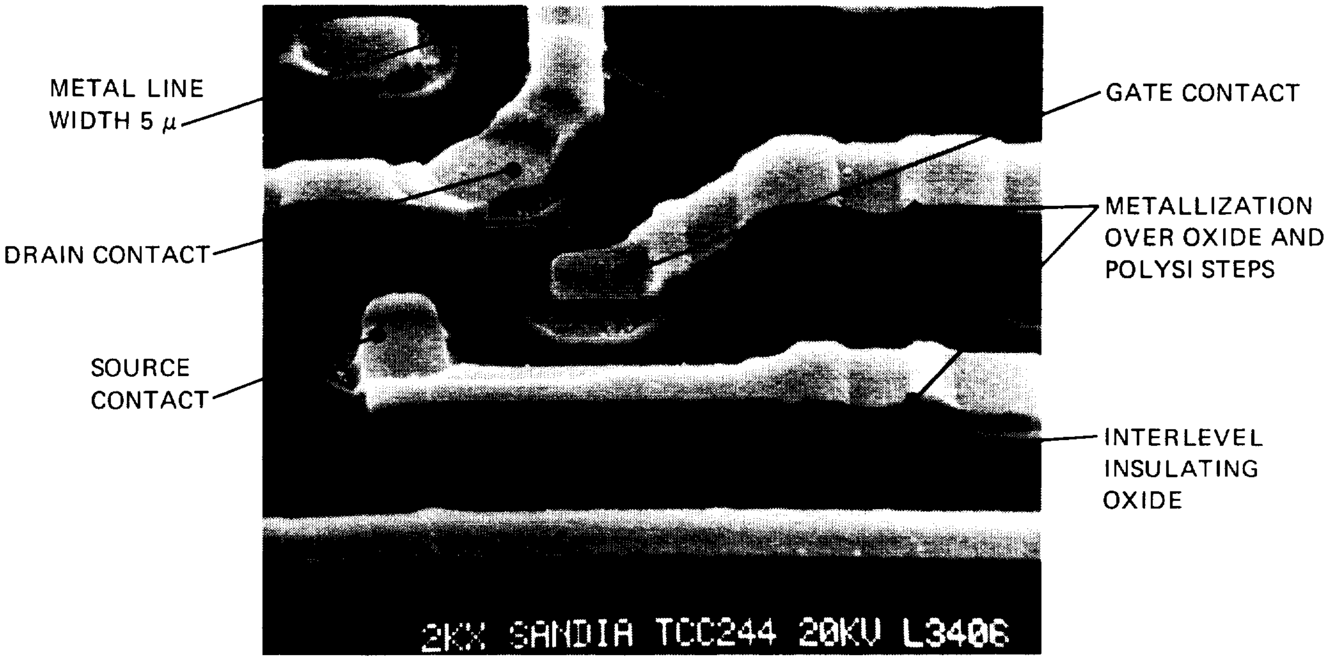


Figure 4-13. (Passivation removed.) 2000x SEM view of N-channel transistor, metal to source, gate and drain interface and step coverage over oxide and polysi steps. (Ref. Fig. 4-10).

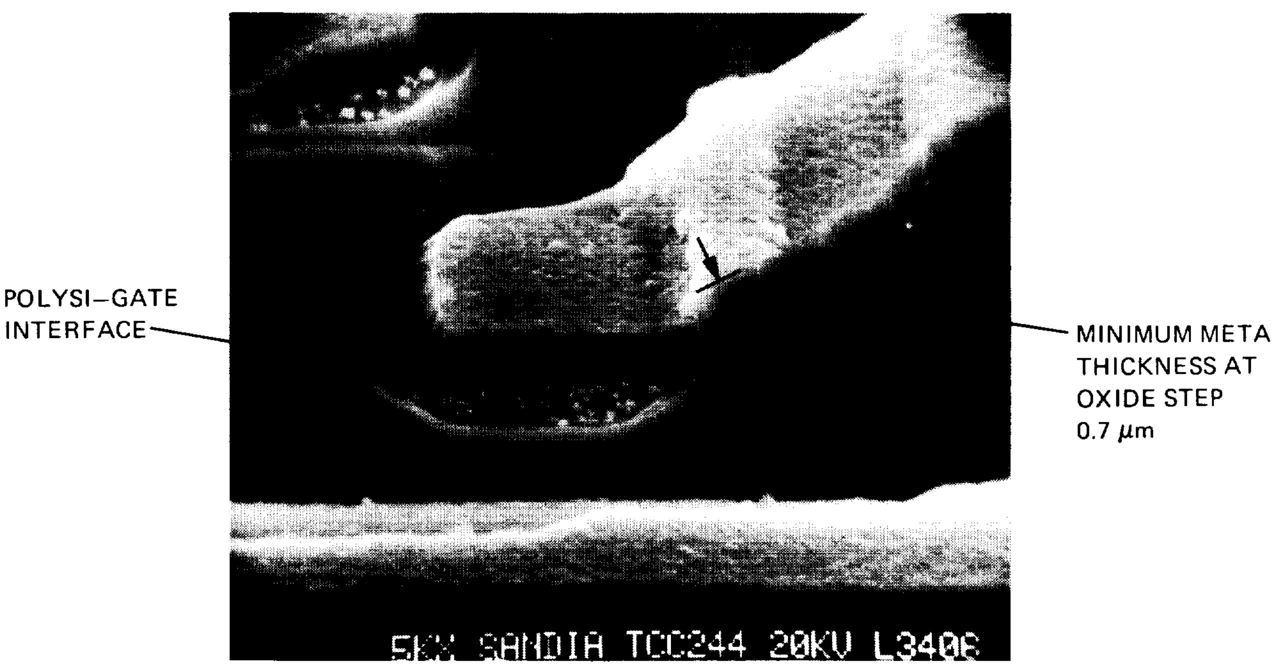


Figure 4-14. 5000x SEM view at 60° tilt of metal step coverage at oxide steps and contact interface to polysi-gate. (Ref. Fig. 4-13.)

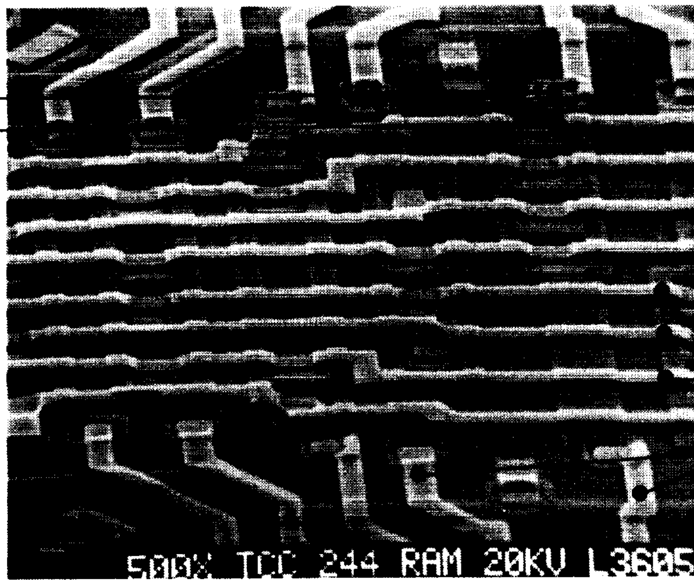


Figure 4-15.

(Passivation removed.) SEM view of word decoder segment, P-channel cells with multiple C^2L polysi-gates and metal address lines. Metal step coverage over oxide insulated polysi-gates.

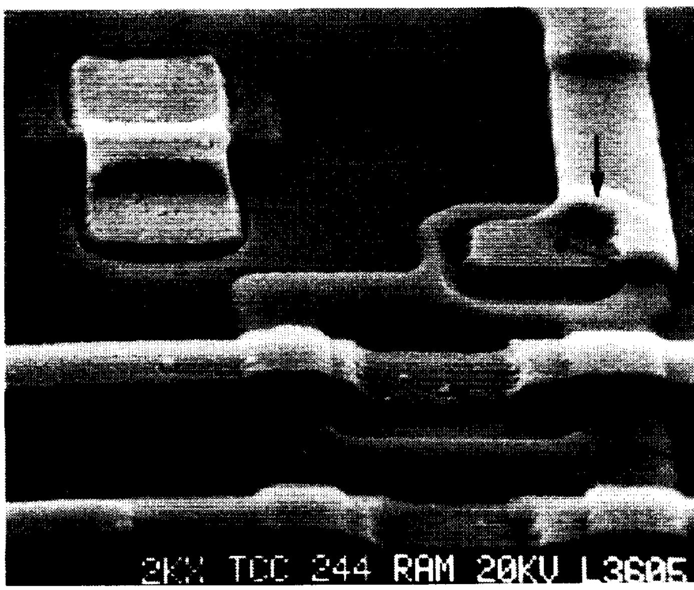


Figure 4-16.

2000x magnified SEM view at 60° of one input address line, metal to polysi interface. (Ref. Fig. 4-15.)

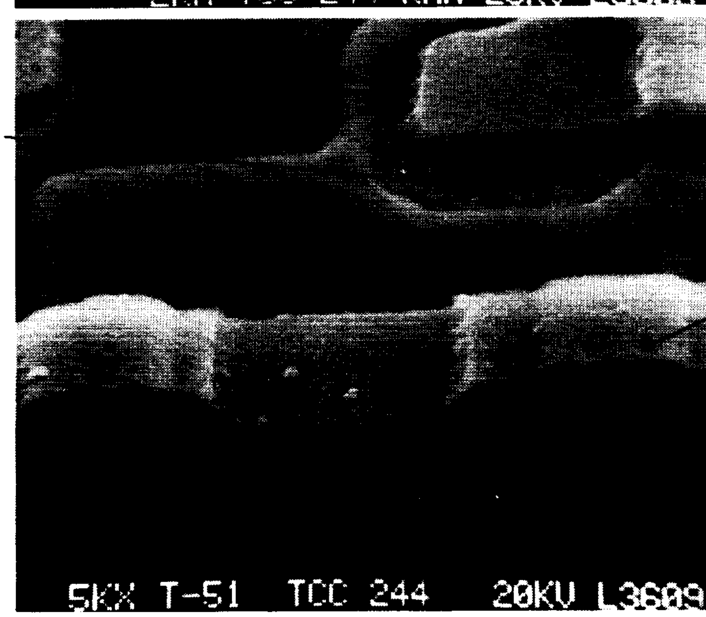


Figure 4-17.

5000x SEM view (Ref. Fig. 4-16) of gate and drain contacts and metal step coverage with side view thickness.

4.3 STEP 2: SEM EXAMINATION AFTER (Aℓ) INTERCONNECT REMOVAL (EXPOSING INTERLEVEL OXIDE, CONTACT APERTURES TO POLYSI-GATES AND SILICON DIFFUSIONS)

The interlevel insulating oxide is exposed and contact window apertures to polysi-gates, P^+ and N^+ cell diffusions.

Magnified optical photo in Figure 4-18 shows the chip with metallization exposed and outline of cell patterns and contacts in oxide. SEM Figures 4-19 through 4-26, together with captions, identify in various positions and magnifications certain circuit segments (some of which may be cross-compared with similar figures in previous step.

The circuit segments with the exposed oxide insulation show and identify the replicating interconnect paths where metal was present, with relatively thin undercut in the oxide due to prior etching step of top SiO_2 passivation (Figure 4-20). The apertures of contact windows with the exposed polysi-gate, P^+ and N^+ cell diffusions contacts area interface are prominently defined in the window perimeters and the sidewall step and depth of insulating oxide (Figures 4-23, 4-25 and 4-26).

Examples of exposed butting contacts of N^+ source plane to P-well are shown in Figure 4-22 and another type butting contact of a polysi field-shield to P^+ source plane in Figure 4-25.

4.3.1 SUMMARY

This level of materials exposure provides important insight into the features of polysi and silicon interface in the exposed contact apertures and about the integrity of insulating oxide that separates now removed top aluminum interconnect. The oxide features and thickness, viewing the sidewall steps at the exposed contacts appear to be uniformly thick layer, approximately 8000 Å on top of polysi and silicon.

The sloping features of oxide steps over polysi-gate patterns were also found to be uniform and without apparent flaws or contaminants.

The features of contact area surface of polysi-gates, P^+ and N^+ cell diffusions in silicon do not exhibit signs of alloy pits, just clean and well defined interface.

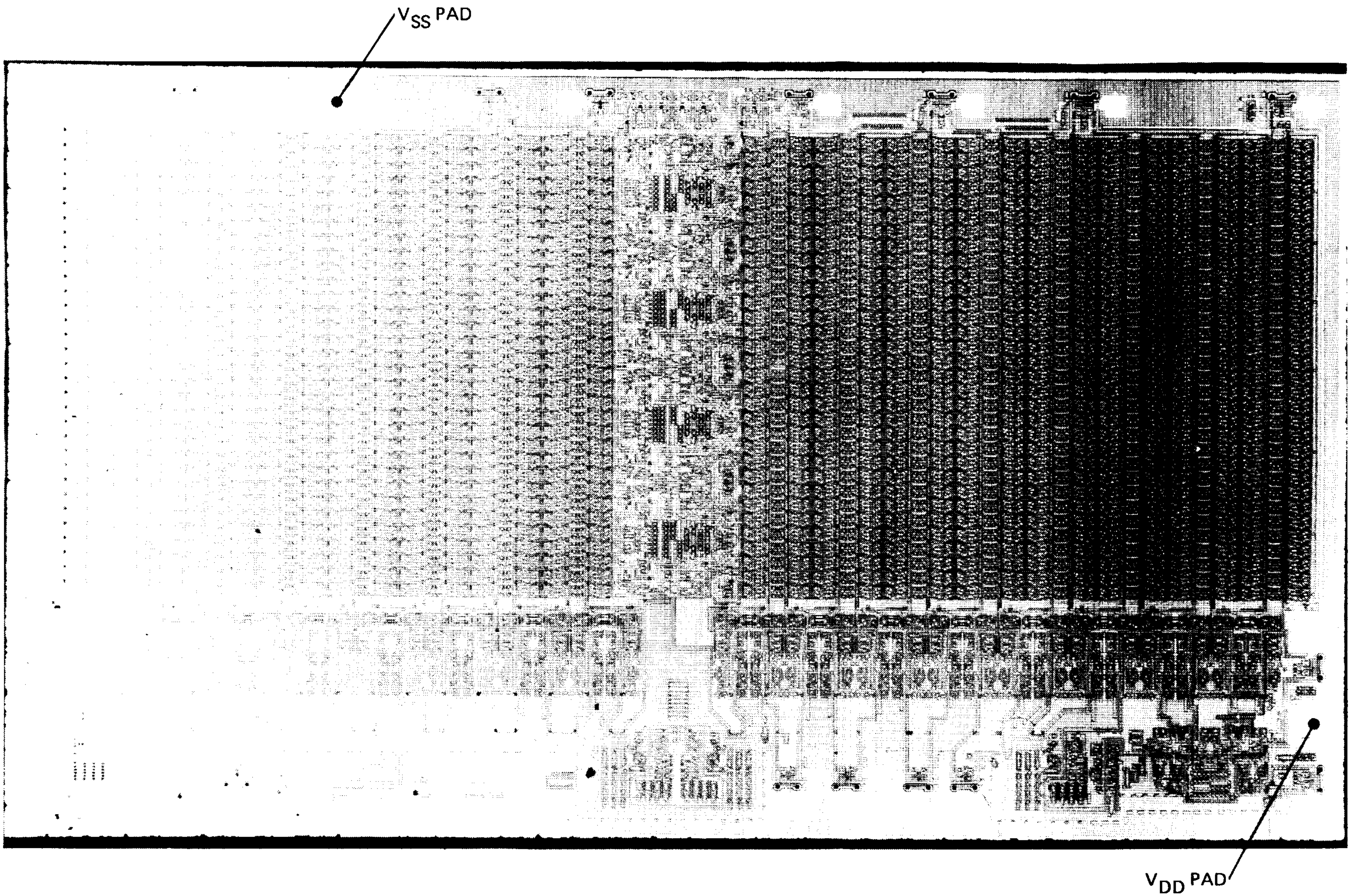


Figure 4-18. Magnified optical view of TCC 244 chip with exposed interlevel oxide and contact apertures to polysi and diffusions. (Top passivation and metal removed.)

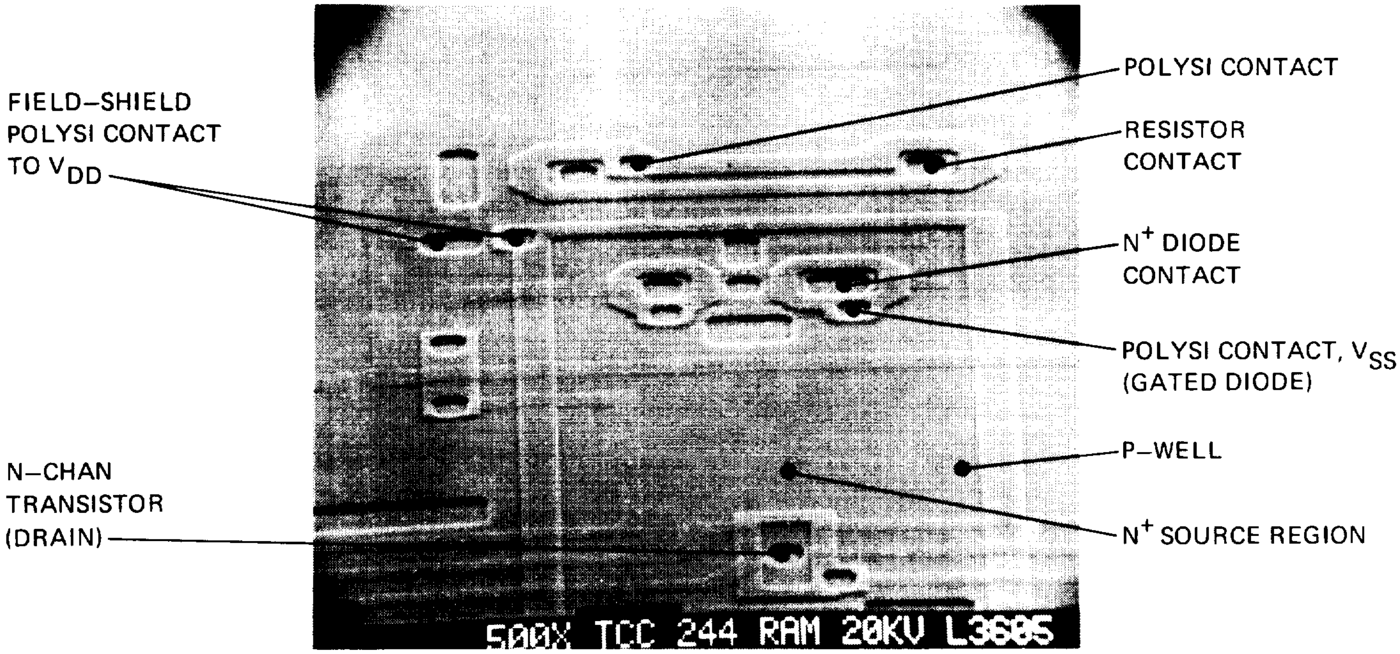


Figure 4-19. (Metallization removed.) 500x SEM view of polysi-gated input protection resistor and two diodes and N-channel transistor with exposed contact apertures in interlevel oxide to polysi and diffusions.

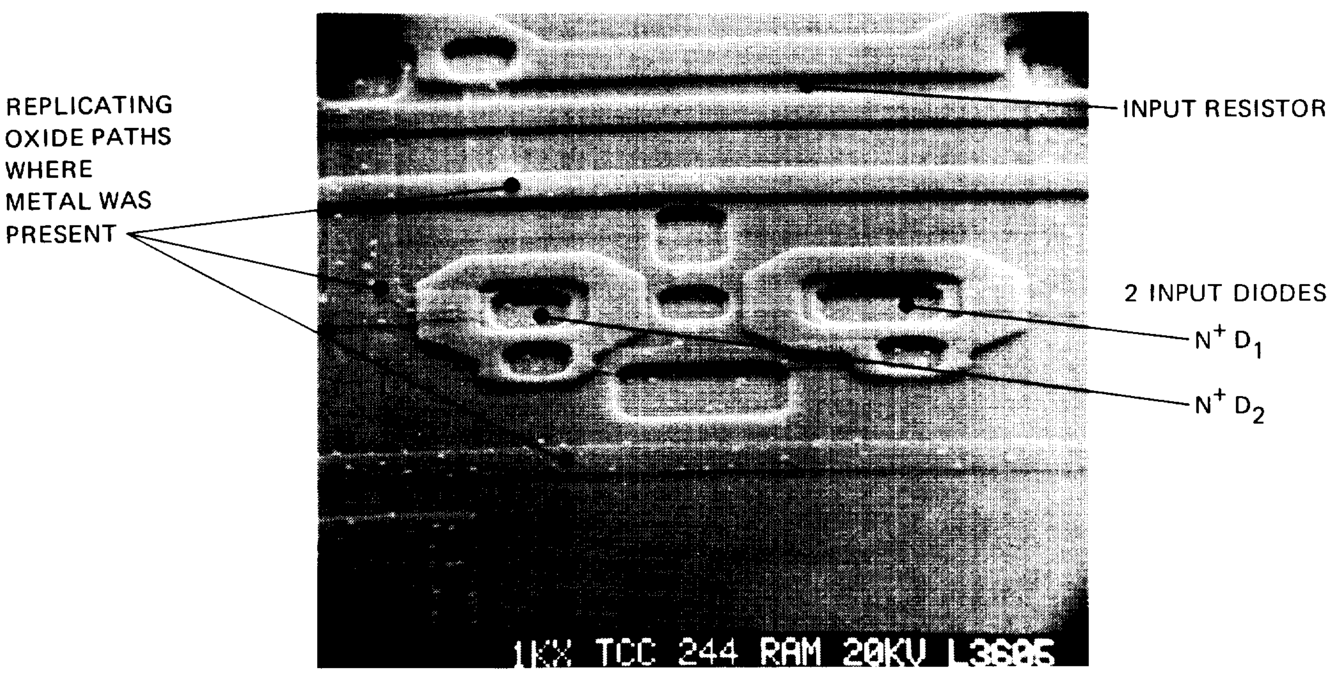


Figure 4-20. 1000x SEM view of two polysi-gated input diodes, exposed contact apertures in interlevel and field oxide to polysi and diffusions., and replicating interconnect paths in oxide where metal was present. (See Fig. 4-8.)

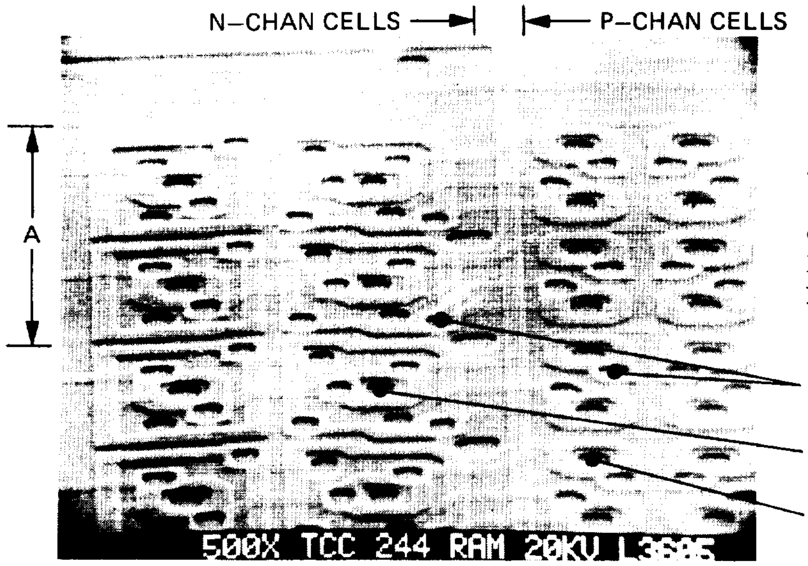


Figure 4-21.

(Metallization removed.) SEM view segment of memory array with four 6-transistor memory cells. Note exposed contact apertures in interlevel oxide to polysi-gates, P^+ and N^+ diffusions.

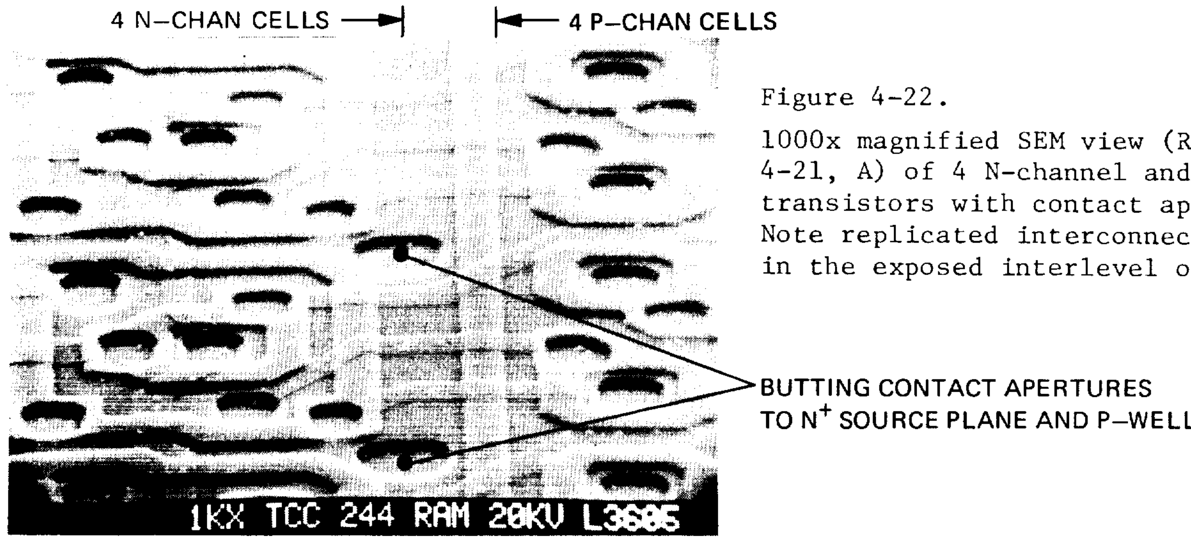


Figure 4-22.

1000x magnified SEM view (Ref. Fig. 4-21, A) of 4 N-channel and P-channel transistors with contact apertures. Note replicated interconnect paths in the exposed interlevel oxide.

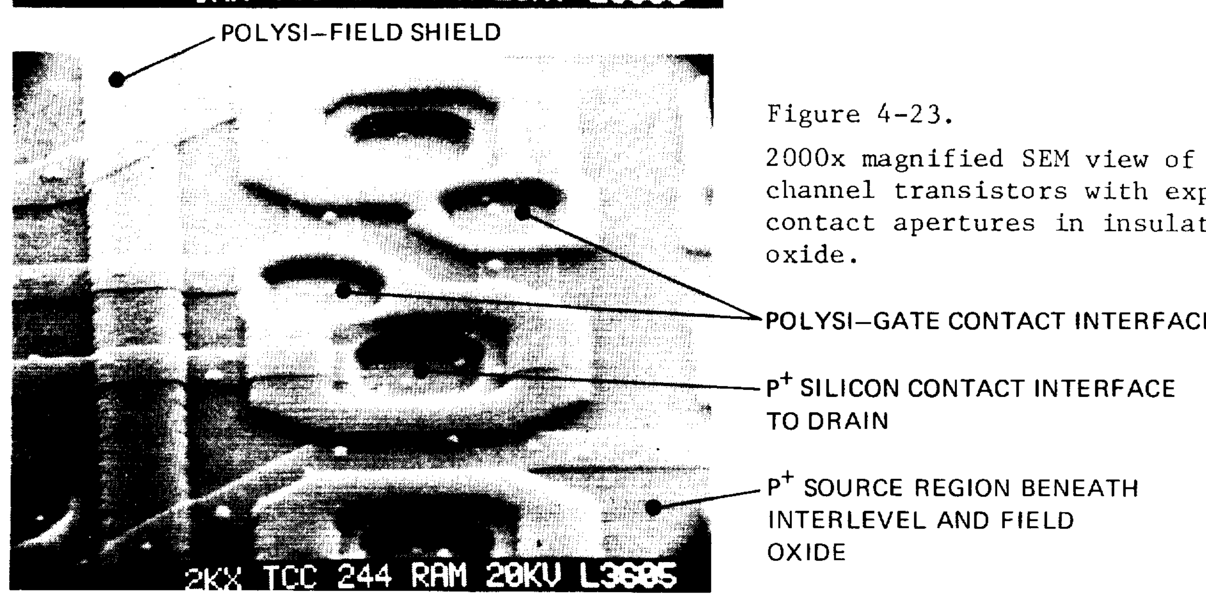


Figure 4-23.

2000x magnified SEM view of 2 P-channel transistors with exposed contact apertures in insulating oxide.

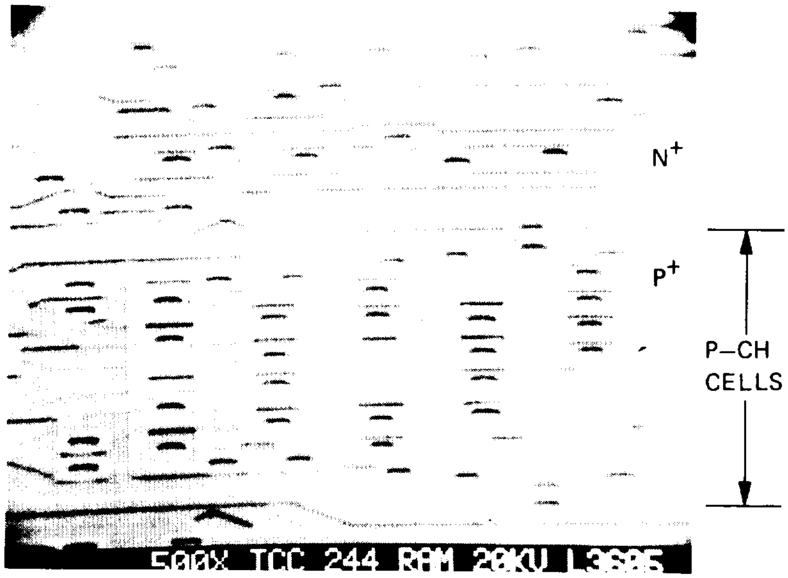


Figure 4-24.

(Metallization removed.) SEM view of word decoder segment P-channel and N-channel cells (60° tilt) with exposed contact apertures. Note multiple drain contacts within rectangular gate patterns, compare with Fig. 4-15.

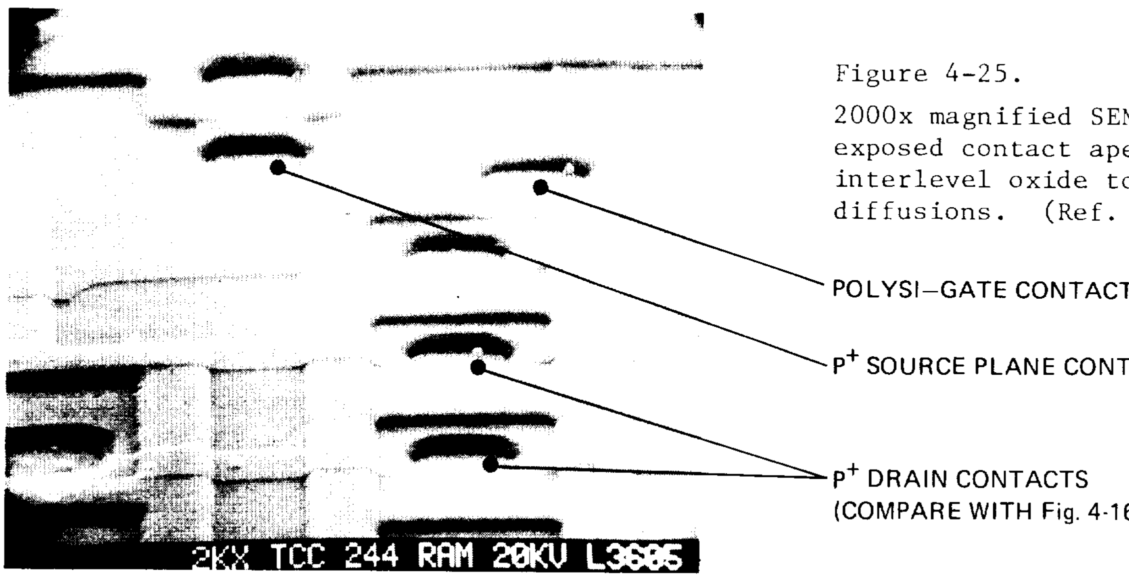


Figure 4-25.

2000x magnified SEM view of exposed contact apertures in interlevel oxide to polysi and diffusions. (Ref. Fig. 4-24.)

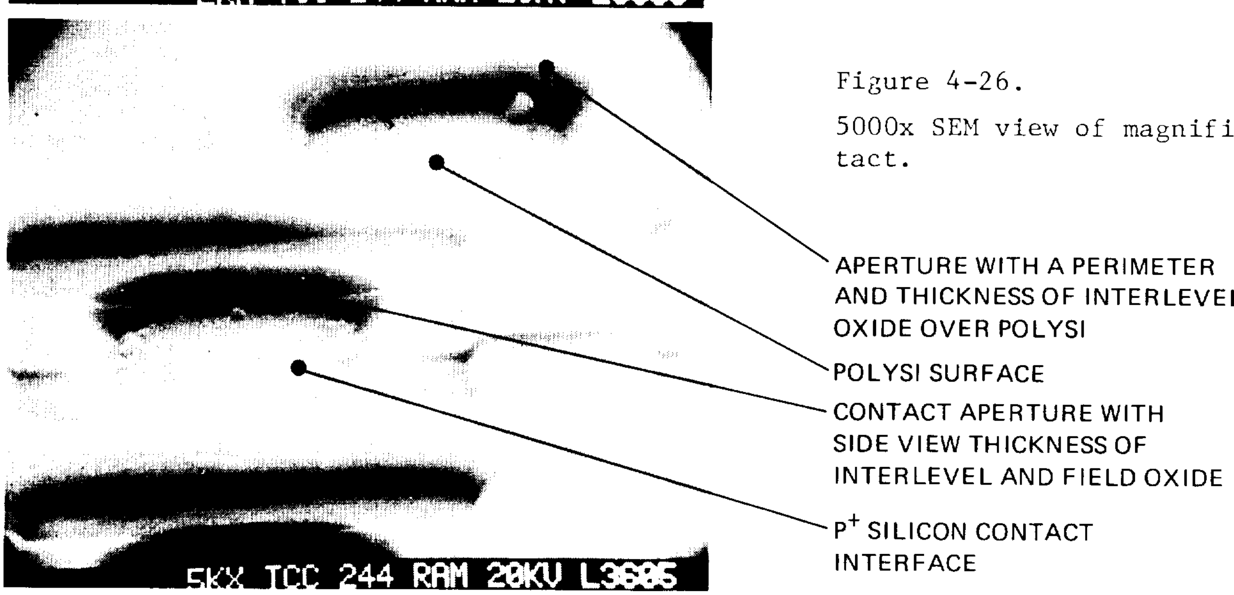


Figure 4-26.

5000x SEM view of magnified contact.

4.4 STEP 3: SEM EXAMINATION AFTER REMOVAL OF INTERLEVEL SiO_2 INSULATING OXIDE EXPOSING POLYSILICON-GATES FIELD SHIELDS AND DIFFUSION PATTERNS

After removal of the interlevel oxide, magnified optical photo Figure 4-27 of the chip displays a good outline of exposed polysi gates with complementary P-channel and N-channel cell patterns of memory matrix, decoders, column sense amplifiers and tri-state output buffers.

SEM Figures 4-28 through 4-37, together with captions, identify in various tilt positions and magnifications similar circuit segments examined in previous steps for cross-comparison at this level of materials exposure. The exposed bare polysi gate patterns in SEM magnification are sharply defined. Polysi rectangular gates with slanted-edge patterns correspond closely to the examples shown in the previous step with oxide coverage (SEM Figures 4-25 and 4-26). The slanted step features of polysi gates helps to reduce the steepness of the oxide step and of top metallization (Figures 4-32 and 4-33).

4.4.1 SUMMARY

The line width of the rectangular polysi-gate is approximately 4.5 μ, with the exception of the gate segment of contact area interface which is more than twice as wide. Unlike in other CMOS processes where the extended polysi contact interface segment lays typically on thick field oxide, with the channel part of a polysi-gate of uniform pattern in the active diffusion over thin channel oxide, this C^2L process lays the entire gate pattern on thin channel oxide and the channel length uniformity is thus not well defined.

The N^+ source planes with N-chan cells within each P-well can be easily identified since each P-well is surrounded by polysi, gate-type, field-shield tied to V_{DD} bus potential. The P^+ source plane with P-chan cells does not have any shielding and P^+ source plane interfaces with N-substrate V_{DD} bus. Examination of P^+ and N^+ silicon contact areas at this level of materials exposure did not reveal any process anomalies.

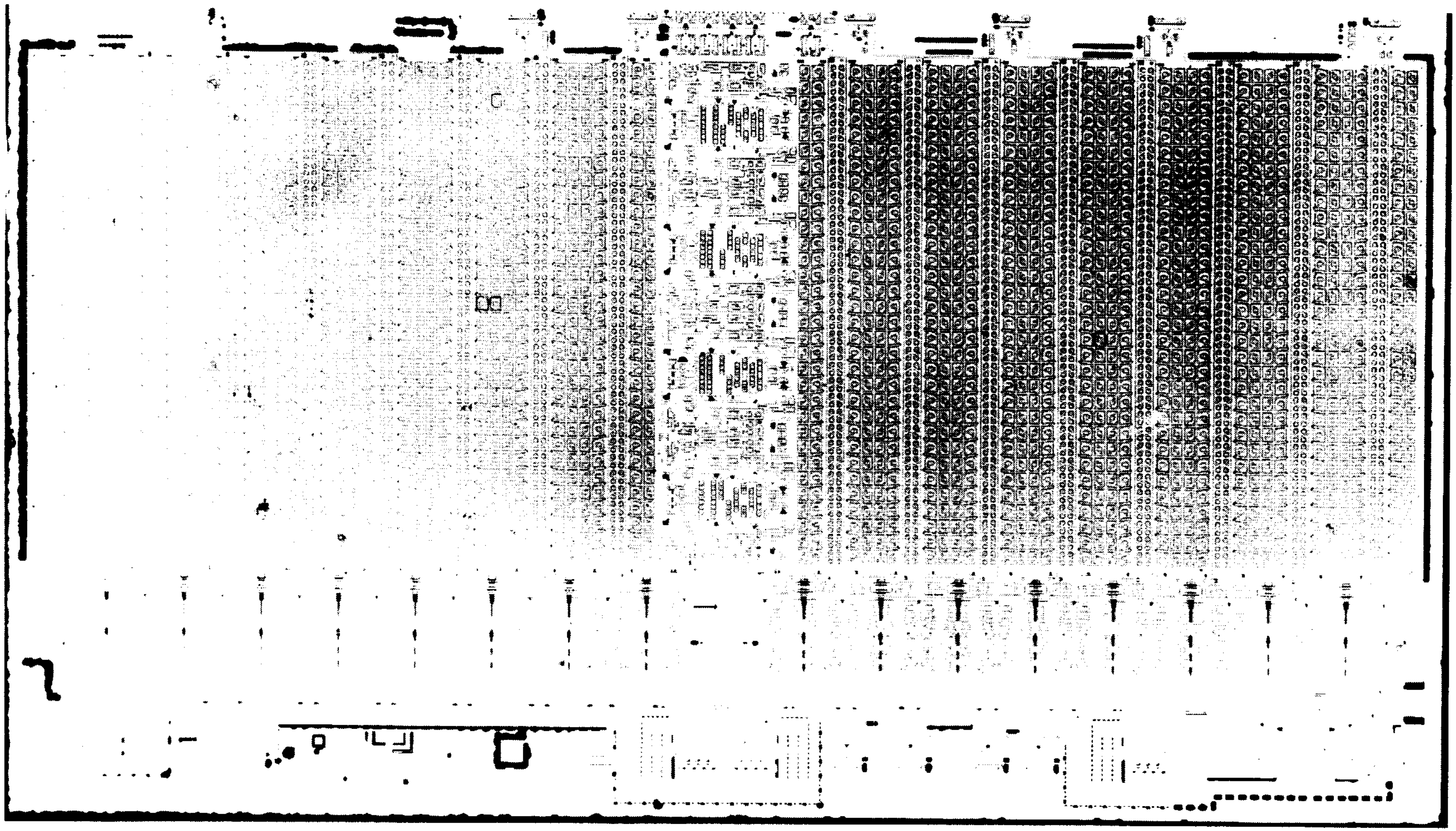


Figure 4-27. Magnified optical view of TCC 244 with exposed polysi-gates, polysi-field shields and contacts to cell diffusions (interlevel oxide removed.)

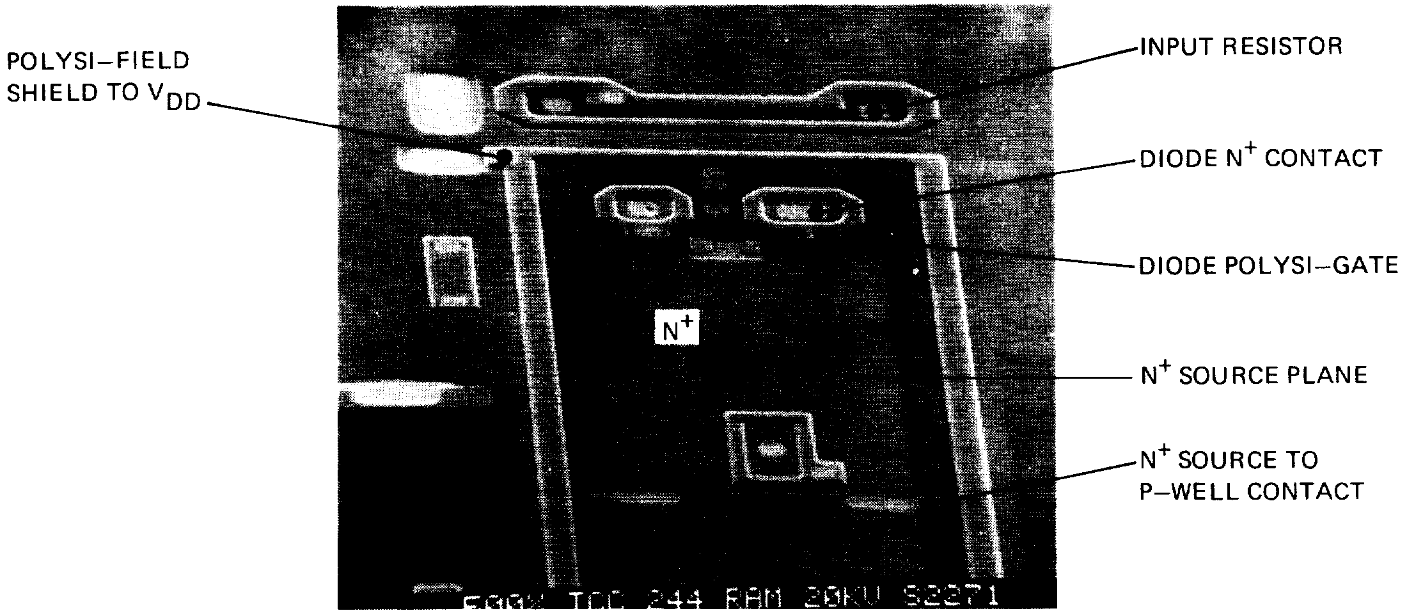


Figure 4-28. (Interlevel oxide removed.) 500x SEM view of input protection resistor, two polysi-gated input diodes and N-channel transistor. Note outline of N^+ source plane within a P-well.

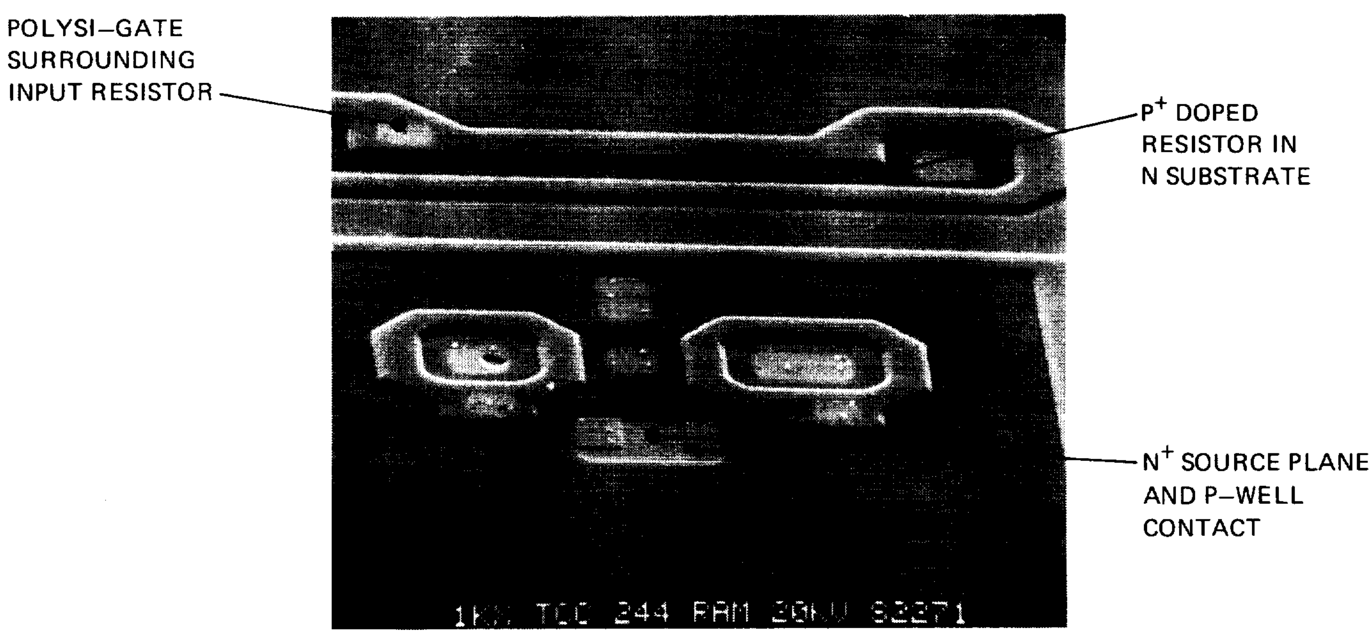


Figure 4-29. 1000x SEM view of exposed polysi-gate pattern of input protection resistor and two diodes.

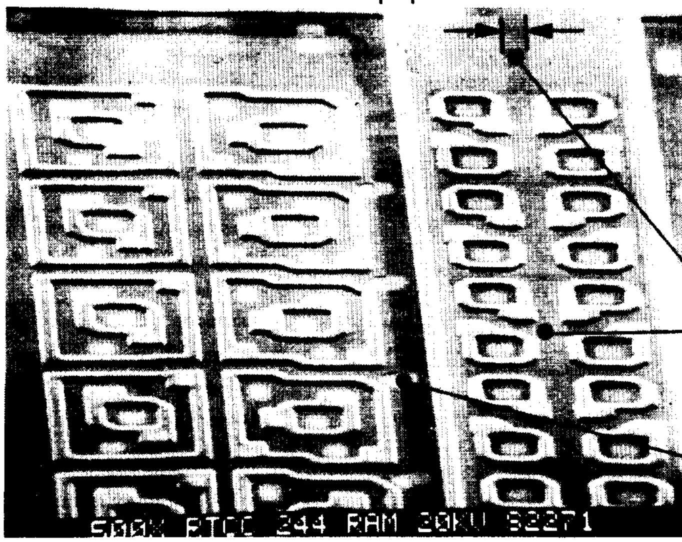


Figure 4-30.

(Interlevel oxide removed.) SEM view segment of memory array with four (6-transistor) memory cells, exposed C^2L polysi-gates rectangular patterns. (Compare with Figs. 4-10 and 4-21.)

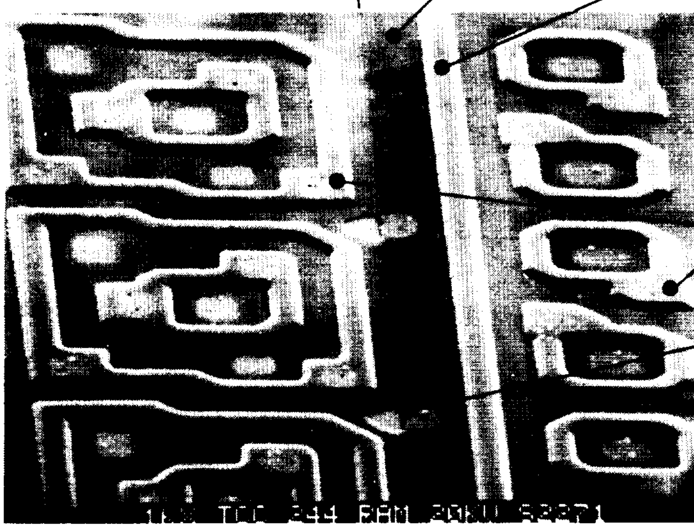


Figure 4-31.

1000x SEM view of bare polysi-gates in N^+ and P^+ regions. (Ref. Fig. 4-30.)

Figure 4-32.

2000x magnified SEM view of bare polysi-gates in P^+ region.

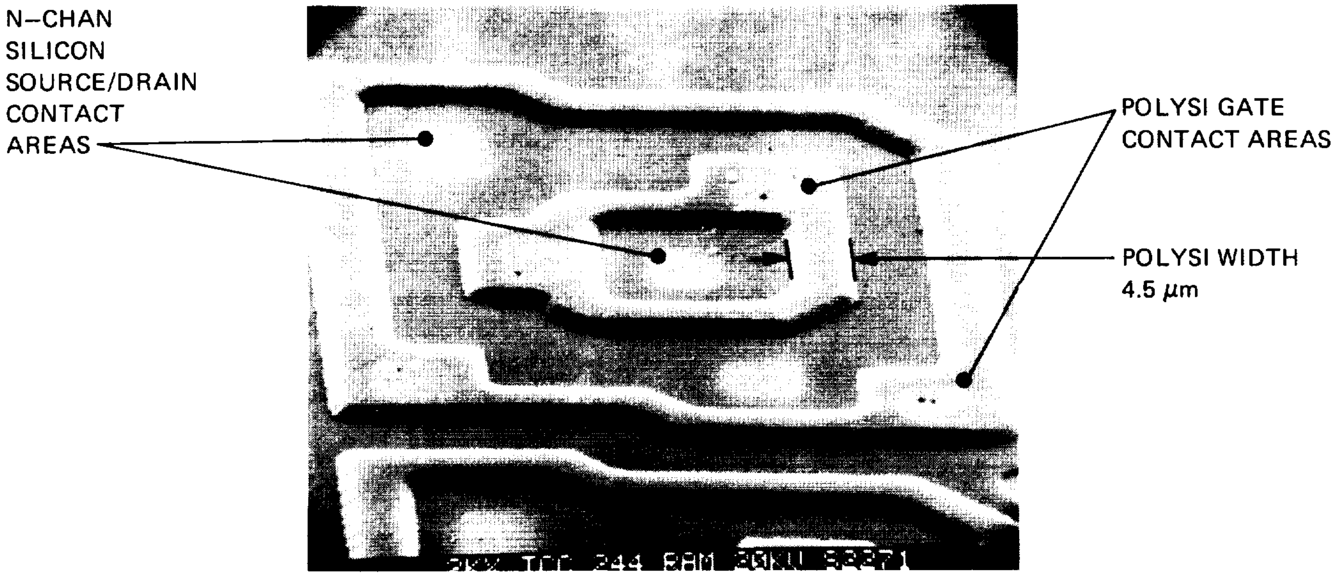


Figure 4-33. (Interlevel oxide removed.) 2000x magnified SEM view of exposed two polysi-gates N-channel cell. Note contact interface areas on polysi surface and in silicon.

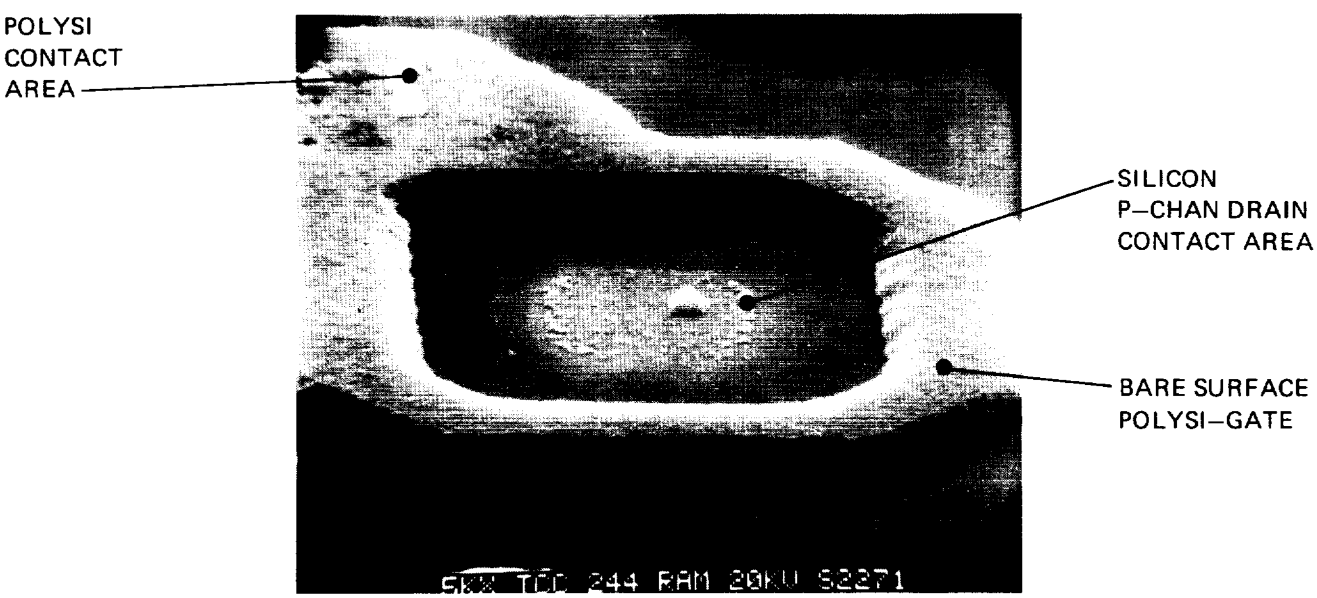


Figure 4-34. 5000x SEM view of P-channnel bare polysi-gate. Note the surface and sloping of polysi pattern and silicon surface of drain contact.

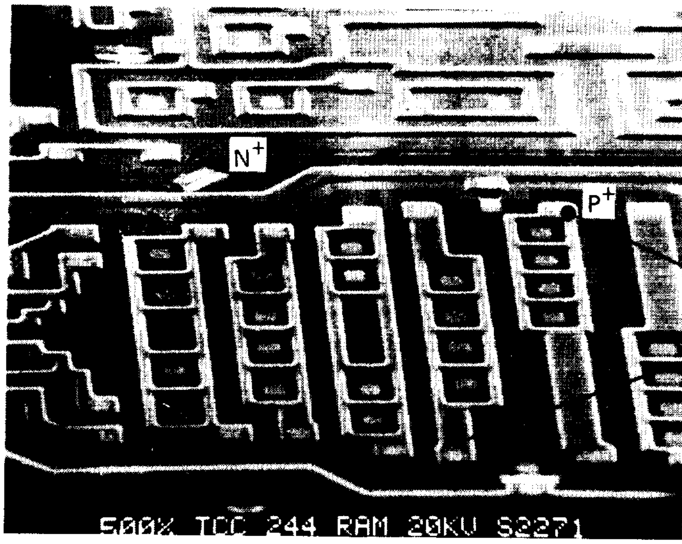


Figure 4-35.

(Interlevel oxide removed.) 500x SEM view of word decoder segment P-channel and N-channel gates. (Ref. Fig. 4-24.)

MULTIPLE P–CHAN POLYSI–GATES;

POLYSI–GATES WITH 4 SEPARATE DRAINS WITHIN

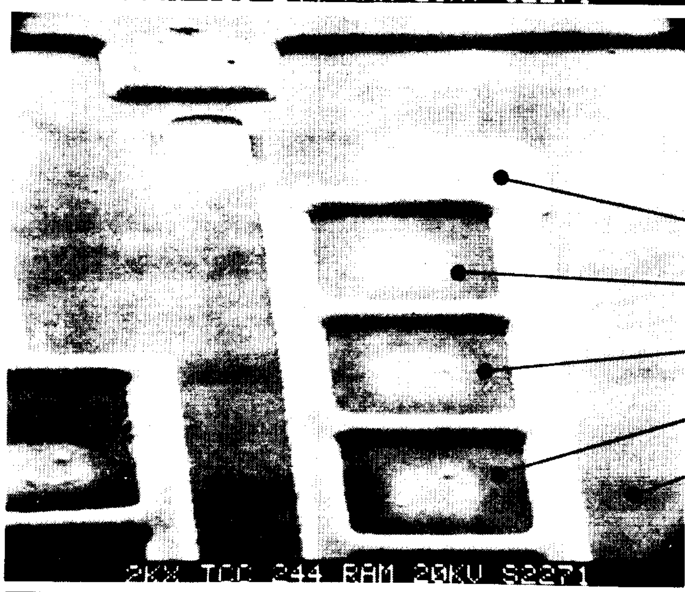


Figure 4-36.

2000x magnified SEM view of bare polysi-gate segment showing three drains. (Ref. Fig. 4-35.)

POLYSI GATE CONTACT AREA

DRAIN NO. 1

DRAIN NO. 2

DRAIN NO. 3

COMMON P^+ SOURCE PLANE

(See Fig. 4-15.)

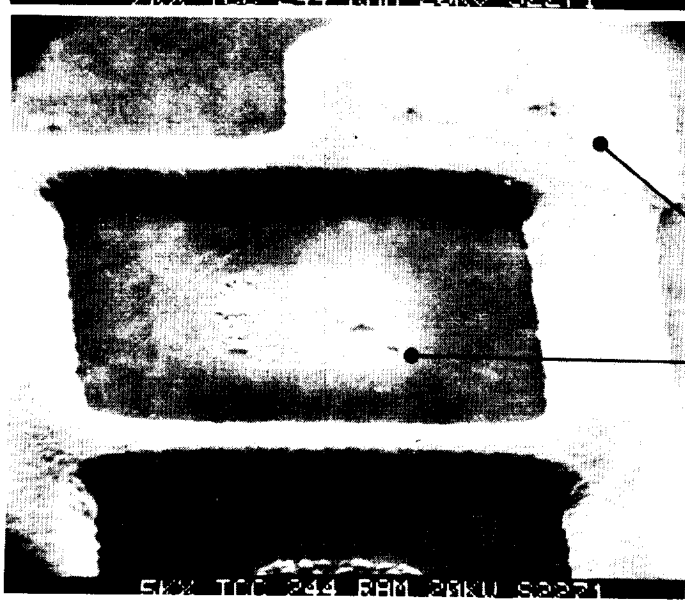


Figure 4-37.

5000x magnified SEM view of bare polysi-gate segment. (Ref. Fig. 4-36.) Note sloping edges and clean polysi-gate pattern and width.

POLYSI GATE CONTACT AREA

1 OF 4 DRAIN CONTACT AREAS IN SILICON

(See Fig. 4-26.)

4.5 STEP 4: SEM EXAMINATION AFTER REMOVAL OF POLYSILICON GATE PATTERNS AND THIN OXIDE

SEM examination of exposed silicon substrate, with P^+ and N^+ source planes and replicating channel patterns outlined in silicon where polysi-gates were present prior to removal, is shown in SEM Figure 4-38 at 500X in a segment of 6-transistor memory cell. The specific reaction of H-F etchant etching into each implanted doping pattern of silicon defined quite accurately the N^+ source plane perimeter and P-well and the P^+ source plane perimeter with a narrow P^+ terminating pattern to V_{DD} bus.

SEM Figure 4-39 shows a 1000X magnified P^+ source segment (ref Figure 4-38) with a better detail of channel patterns in silicon and apparently few pin-hole anomalies in channel path outlines in the areas, vertically above, of polysi-gate contact interface, now removed.

SEM Figure 3-40 shows a magnified N^+ source plane segment with channel patterns in silicon and identifies the details in the caption.

4.5.1 SUMMARY

The examples of channel outlines of the exposed silicon surface morphology appear to verify that the polysi-gates with contact terminations are on the same thin gate-oxide. The approximate 750 Å thickness of this oxide is what separates the top metal contact interface to all polysi on this chip. Taking into consideration the sintering effect for polysi to metal contact interface which might be a cause of pinhole defects, shown in Figures 4-39 and 4-40. Further evaluation of pinhole anomaly is suggested together with electrical tests for oxide breakdown integrity and potential current leakage (at elevated temperatures) between V_{SS} and V_{DD} bus.

THREE EXAMPLES OF EXPOSED SILICON SUBSTRATE OF 6-T MEMORY CELL

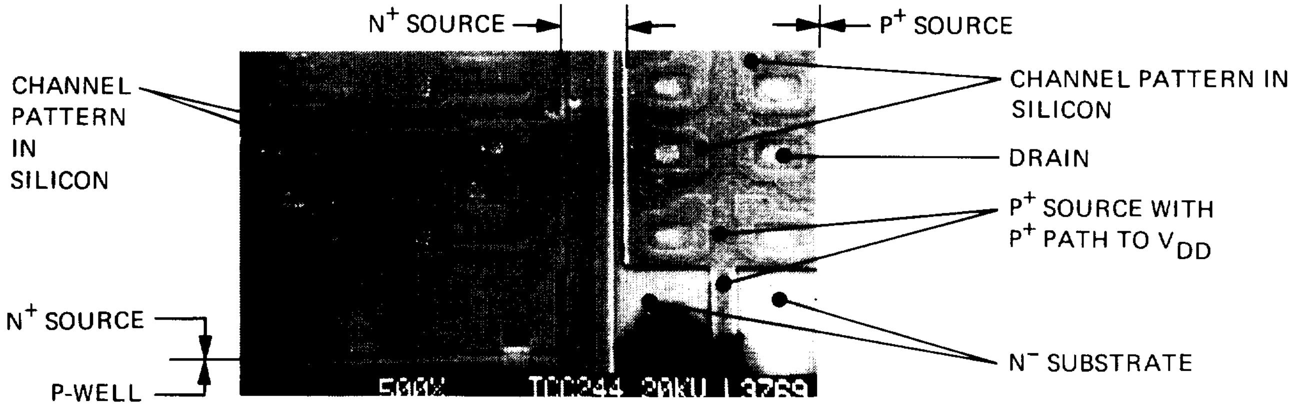


Figure 4-38. SEM view of 6T memory cell pattern in silicon diffusions.

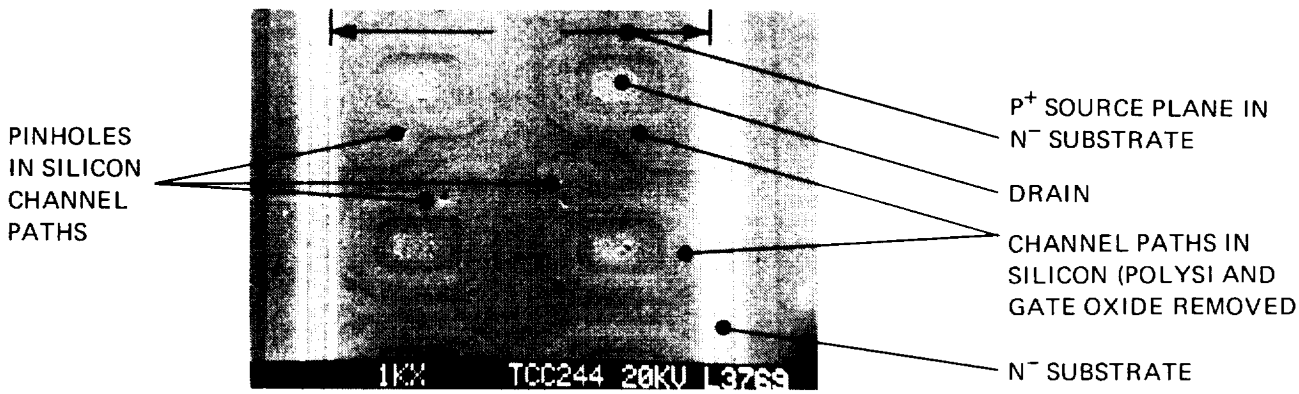


Figure 4-39. 1000x SEM view of P^+ segment, ref. Figure 4-38 above.

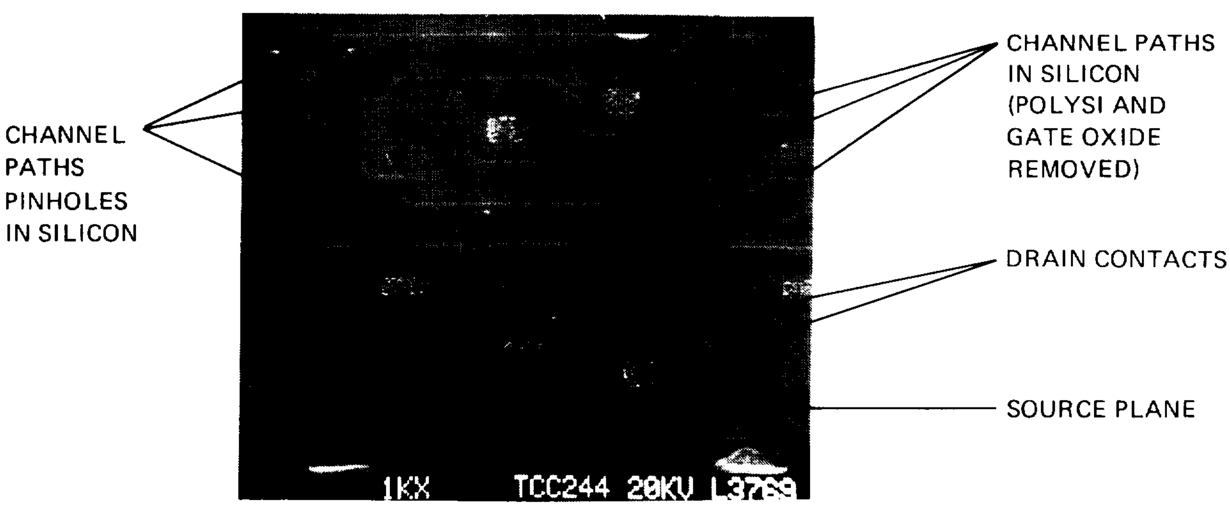


Figure 4-40. 1000x SEM view of N^+ segment, ref. Figure 4-38 above.

4.6 CROSS-SECTIONING OF TCC 244 CHIP

A cross-section of a chip was performed on a standard polishing and lapping system in two steps, A and B.

Step A was to approximate vertical definition (thickness) of chip surface materials (e.g., top passivation metallization, interlevel oxide, and polysi gates with channel oxide).

Step B subsequently defines, by staining the junction depth, effective channel length in silicon together with polysi-gate length and gate oxide in channel path.

Example A in SEM Figures 4-41a, 4-41b and 4-41c show a cross-section sample with passivation, metallization, interlevel insulating oxide and polysi gates on silicon substrate with channel oxide.

Example B in SEM Figures 4-42a, 4-42b and 4-42c show a cross-section sample, after staining with interlevel oxide, polysi and junction definition in silicon substrate.

The SEM Figures together with explanatory captions provide an insight into cross-sectioned materials and dimensions.

4.6.1 SUMMARY

This was a single attempt to prepare a cross-section for this report only, and not an extended cross-section sampling of several chips. Therefore, these results may not provide more complete details of many samples. Significant is the patterning of polysi gates with sharply slanted slopes which reduce channel length in silicon due to implant step affected by thin gate-polysi edges on both sides, and this makes the polysi-gate length wider. In effect, this helps in following steps of interlevel oxide deposition showing uniformly sloping step thickness at the polysi steps which, in turn, again help in metallization step coverage (SEM Figures 4-41c, 4-42b and 4-42c).

The P^+ diffusions depths in silicon as well as approximation of channel oxide thickness and polysi may be fairly well estimated from SEM figure magnification factor together with use of a metric ruler (in mm).

EXAMPLES OF CROSS-SECTION SEGMENT AT 90° OF PASSIVATED TCC 244 CHIP WITH PATTERN OF POLYSI–GATES, INTERLEVEL OXIDE, METAL INTERFACE TO SILICON.

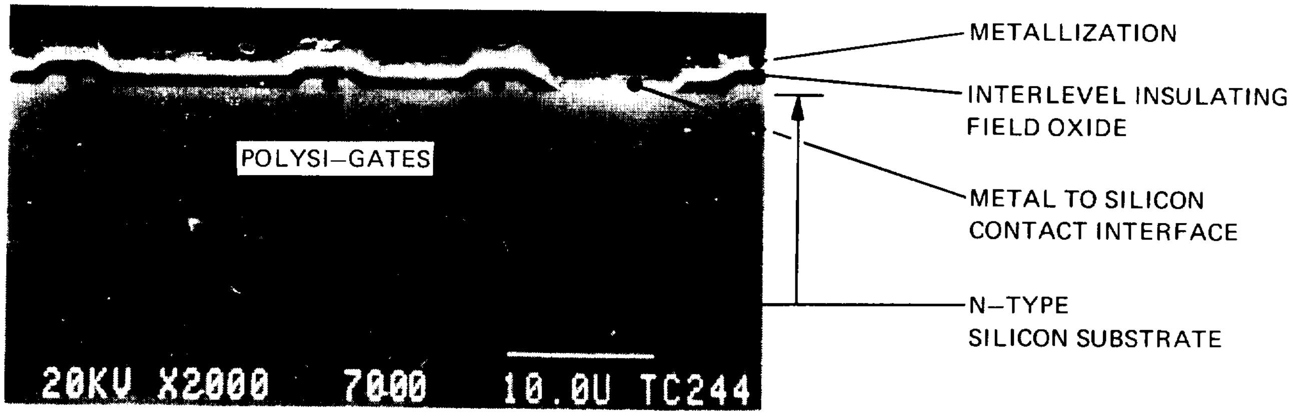


Figure 4-41a. 2000x magnified SEM view cross-section of polysi-gates, interlevel oxide, metallization and silicon substrate.

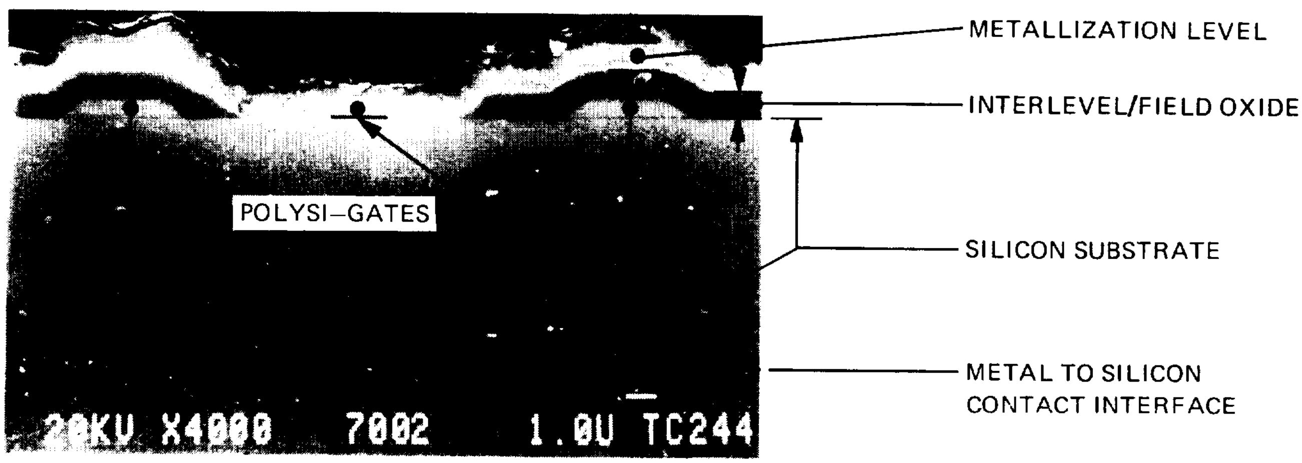


Figure 4-41b. 4000x SEM view of cross-section, two polysi-gates, metal to silicon interface.

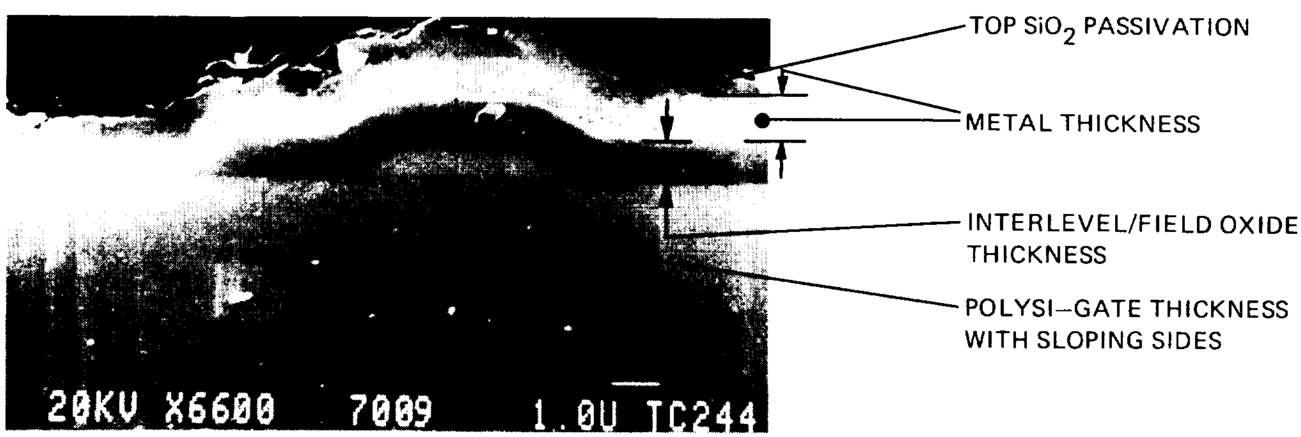


Figure 4-41c. 6600x SEM view of magnified cross-section (Ref. Fig. 4-41 a and b.)

EXAMPLES OF CROSS-SECTION SEGMENT WITH MAGNIFICATIONS, TCC 244 (AFTER STAINING) TO DEFINE P^+ JUNCTIONS DEPTH IN SILICON SUBSTRATE, POLYSI–GATE WITH CHANNEL OXIDE AND CHANNEL PATTERN IN SILICON

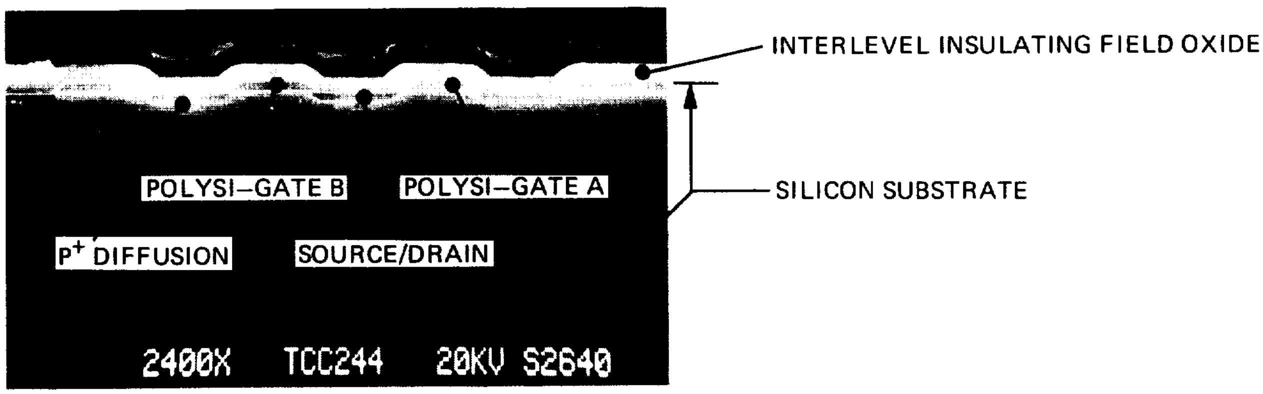


Figure 4-42a. 2400x SEM view of polysi-gates and delineated P^+ diffusion in silicon substrate.

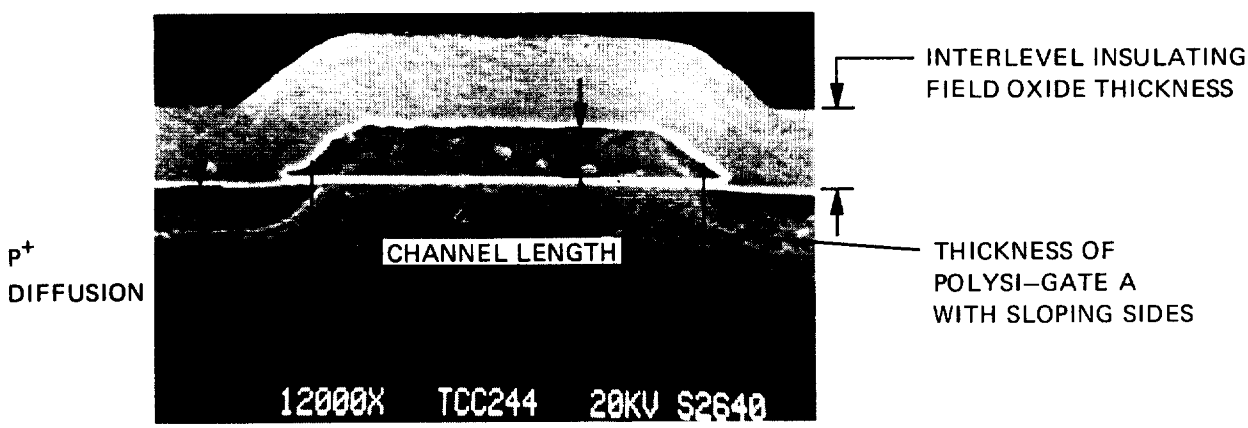


Figure 4-42b. 12000x magnified SEM view of polysi-gate A, channel pattern and P^+ diffusions. (Ref. Fig. 4-42a.)

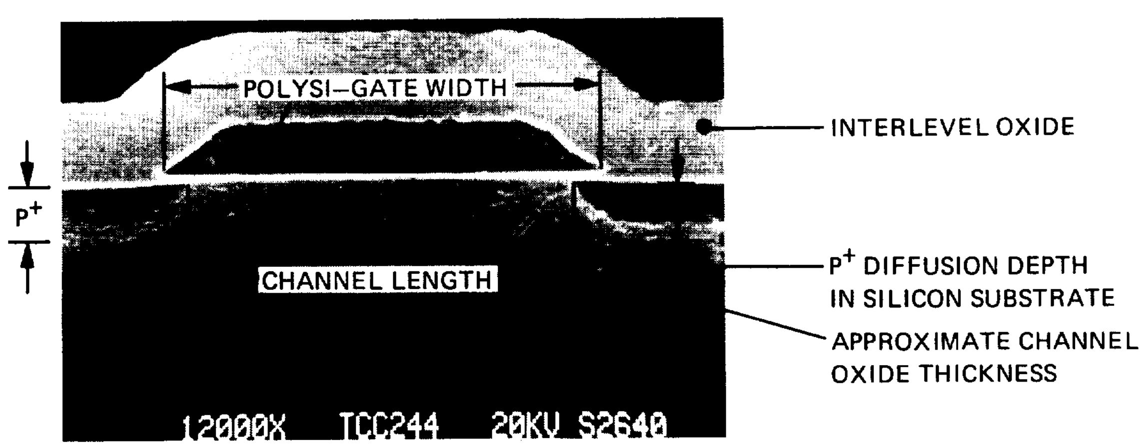


Figure 4-42c. 12000x magnified SEM view of polysi-gate B, channel length in silicon between two P^+ diffusions.

The SEM examples can be compared also with the examples in previous steps, with the exposed polysi and with interlevel oxide to validate the sloping steps of both materials.

SECTION V

PROCESS FABRICATION

5.1 FABRICATION MATERIALS AND PATTERNS

The Sandia TCC 244 (256 x 4) 1K CMOS RAM chip is fabricated on N-type <100> bulk silicon, using RCA developed self-aligned closed polysi-gate called C^2L CMOS technology.

The sequence of process steps derived from observations made through this physical evaluation closely approximates the photo mask steps shown in Figures 5-1 through 5-8. These figures are cross-section diagrams illustrating the process steps which approximately define for this LSI device the C^2L CMOS process technology, also used in the CDP 1800-00 series family of devices. However, the Sandia-made device differs in one respect, compared to standard RCA CDP 1800 device types, in that it is developed with a radiation hardened proprietary process and masking steps.

The chip protective passivation is highly granular and partially opaque SiO_2 passivation with approximate thickness of 8000 Å.

The two types of interconnect on the chip are aluminum and polysi. Except for contact interface these two levels are separated by interlevel insulating SiO_2 with approximate thickness of 8500 Å with good step coverage uniformity over polysi patterns. The interface contact apertures for top metal interconnect to polysi-gates and implanted (P^+, N^+) diffusions in silicon substrate are photomask patterned in the interlevel oxide. (See SEM Figures 4-23 and 4-25, Section IV.)

Typically, the polysi-gate patterns are of rectangular (ring) shape with a contact. The center surrounded by polysi-gate is the "drain" junction area for P- or N-channel transistors. These gate patterns are separated from silicon substrate by gate-oxide with an approximate thickness of 750 Å.

The region outside these polysi-gate (rings) is typically called a source plane. The P^+ source plane on N-substrate accommodates all P-channel transistors. The N^+ source plane within a P-well accommodates all N-channel transistors, also each P-well with N^+ source plane is surrounded by a polysi field-shield equal in pattern to a polysi-gate but with a large perimeter. Each

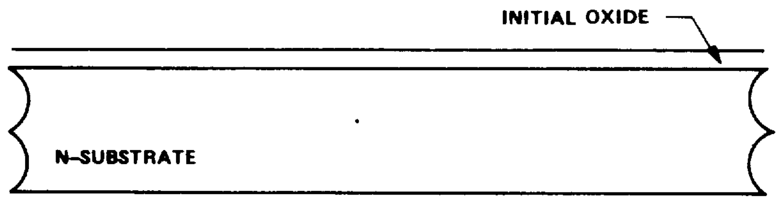


Figure 5-1. Initial oxidation of silicon wafer.

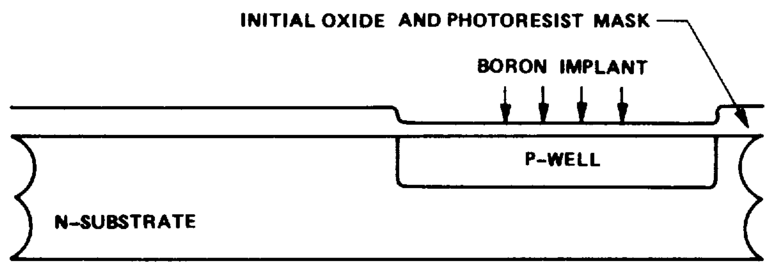


Figure 5-2. Oxidation and photo-resist mask step, defining P-well areas followed by boron implant and diffusion step.

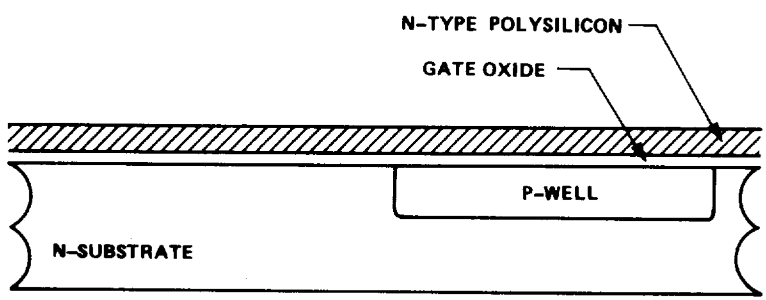


Figure 5-3. Initial oxide and photo-resist removed, followed by grown channel oxide step and deposition of doped polysilicon.

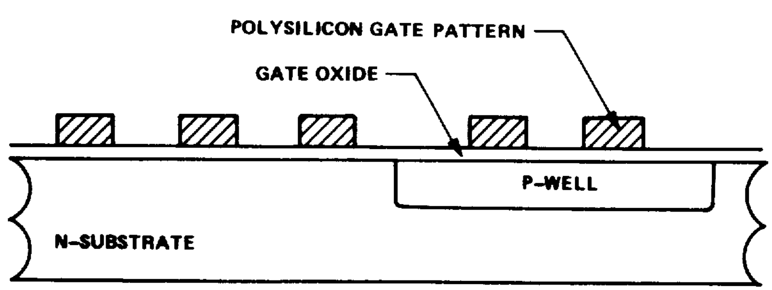


Figure 5-4. Photo-resist mask and etch step defining (C^2L) polysilicon gates, field-shields and interconnect.

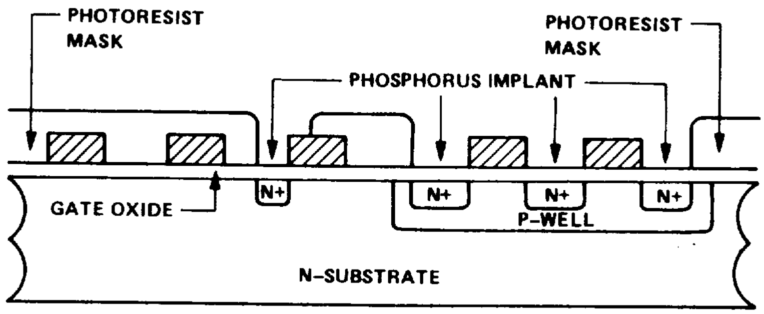


Figure 5-5. Photo-resist mask and etch back step exposing P-wells followed by phosphorus implant step which defines N-channel transistors.

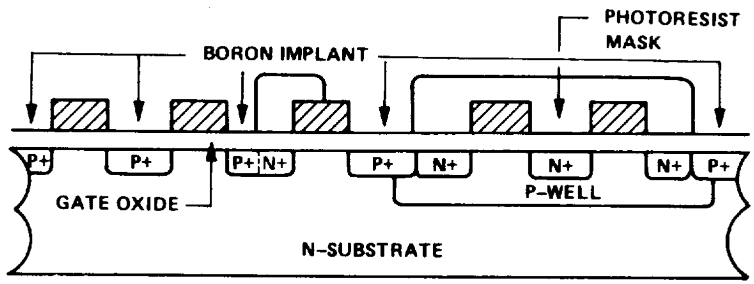


Figure 5-6. Photo-resist mask and etch back step exposing areas for P-channel transistor patterns followed by boron implant.

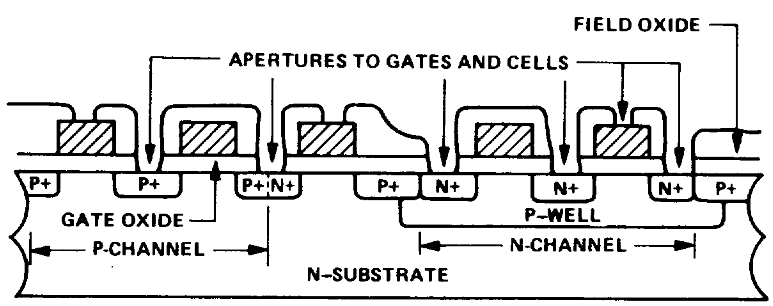


Figure 5-7. Photo mask removed followed by deposition of interlevel oxide and photo-resist mask and etch step defining apertures to polygates, source and drain contacts.

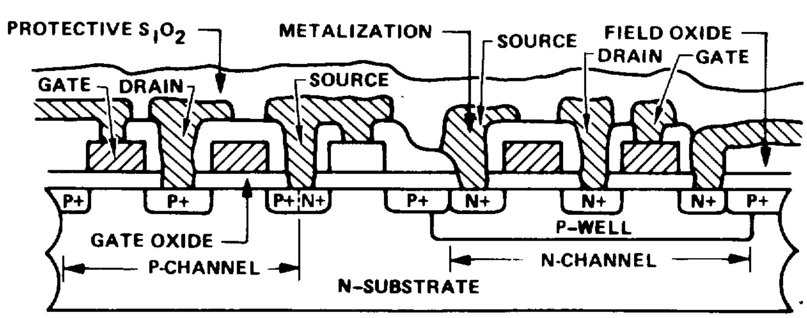


Figure 5-8. Deposition of aluminum followed by photo-resist mask and etch step defining metallization interconnect and subsequent sintering followed by protective oxide deposition and photo-resist mask defining contact areas to chip metal pads and test patterns.

polysi-field-shield surrounding a P-well is tied to V_{DD} bus of P^+ source planes on N-substrate. Each N^+ source plane with butting contacts to P-well is the side of V_{SS} bus.

In addition; other polysi-gated patterns are input protection resistors and diodes. The input protection resistors are boron (P^+) implants in N-substrate surrounded by a polysi gate type pattern on channel oxide, these polysi-gates of resistors are tied to the V_{SS} bus.

The input diodes are placed within a P-well, each one is surrounded by a polysi-gate which is tied to the V_{SS} bus. The center part of each diode is N^+ doped. The third diode in each input protection is a distributed diode of an input resistor.

5.2 SUMMARY

Though the typical width of a polysi-gate is approximately 4.5 μ; estimating the channel length beneath this (irregular) rectangular gate, because of its contact area width on the gate, is not precisely possible.

The sharply slanted slopes of these gates allow for implant doping penetration through the thinner part of polysi slope at the gate-oxide interface and make the channel length in silicon narrower though still irregular because of the polysi pad area width.

The typical C^2L fabricating process requires six photo mask operations. However, because of proprietary radiation-hardened material process requirements, the masking steps and materials processes may vary and would be higher.

5.3 DIE INTERNAL MATERIALS AND DIMENSIONS

Most of these dimensions were derived from approximations from the SEM photos, taking into account the SEM magnification factor and the position of the specimen in the SEM.

Table III. Physical Dimensions and Materials

1.	Die attach material	Gold eutectic
2.	Die size	238 x 138 mils
3.	Silicon substrate	N-type
4.	Die passivation	SiO_2
5.	Passivation thickness	0.8 μ
6.	Die wire bond	1.3 mils
7.	Wire bonding technique (wedge)	Ultrasonic
8.	Die metallization	Aluminum
9.	Typical metallization thickness	1.1 μ
10.	Minimum metal thickness at oxide and polysi steps	0.7 μ
11.	Minimum metal line width	4.7 μ
12.	Minimum metal line separation	7. μ
13.	Typical interlevel SiO_2 insulation thickness	0.9 μ
14.	Typical contact window apertures in SiO_2 to polysi and silicon substrate	6. x 6. μ
15.	Polysi-gate width (channel length)	5.2 μ
16.	Polysi-gate thickness	0.58 μ
17.	Approximate channel length in silicon	4. μ
18.	Approximate P-chan diffusion depth in N-substrate	0.6 μ
19.	Approximate gate-oxide thickness	750 Å
20.	Approximate P-well depth in silicon substrate	10. μ

Die Topography. See ref Figures 3-2 and 3-3 with identified circuit block patterns.

APPENDIX A

ELECTRICAL RATINGS

Absolute maximum electrical ratings.

Storage-Temperature Range (T_{stg})	-65 to +150°C
Operating Temperature Range (T_A)	-55 to +125°C
Supply Voltage Range (V_{DD} - V_{SS})	-0.5 to +12V
Power Dissipation Per Package (P_D):	
For T_A = -55 to +100°C	500 mW
For T_A = +100 to 125°C . . . Derate linearly at 12 mW/°C to 200 mW	
Device Dissipation Per Output Transistor:	
For T_A = -55 to +125°C	100 mW
Input Voltage Range, All Inputs	-0.5 to V_{DD} +0.5 V
DC Input Current, Any One Input	±10 mA
Lead Temperature (During Soldering):	
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max	+265°C
Maximum Junction Temperature (T_j)	+150°C
Thermal Resistance, Junction to case (θ_{JC})	.15°C/mW for flat package

Recommended operating conditions. (At T_A = -55°C to +125°C)

Supply Voltage Range (V_{DD} - V_{SS})	4.5 to 11 V
Input Low (V_{IL}) Voltage Range	0 to 1.5 V at V_{DD} = 5 V 0 to 3 V at V_{DD} = 10 V
Input High (V_{IH}) Voltage Range	3.5 V to 5 V at V_{DD} = 5 V 7 V to 10 V at V_{DD} = 10 V